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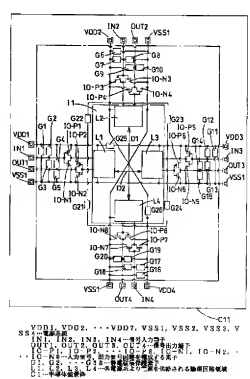
(54)【発明の名称】　半導体装置

(57)【要約】
【課題】少なくとも４系統の電源電圧系統を有する半導体装置において、各電源系間の静電気印可時の耐量を確保する為には静電気電荷の放電経路にある保護素子が多く介在し、また、放電経路の配線寄生抵抗により耐量が下がってしまう、という課題を解決した半導体装置を提供する。
【解決手段】放電経路に通常動作時の電源配線を利用し、また各電源系（例えばＶＤＤ１、ＶＤＤ３）の領域の最も近い領域に保護素子（例えばＧ２５）を配置することにより耐量を確保する。



【特許請求の範囲】

【請求項１】　半導体装置外から前記半導体装置内に電源を供給する複数の電源端子と、

前記電源端子のうち低い電圧を供給する電源端子と他の電源端子との間に介在されてそれぞれ静電破壊電荷から半導体装置を保護する複数の第１の保護素子と、

前記低い電圧を供給する電源端子の相互間に介在されて各々の電源端子に対して静電破壊電荷から保護する複数の第２の保護素子と、

前記他の電源端子および前記低い電圧を供給する電源端子の電圧によってそれぞれ動作する半導体素子により構成される複数の電源電圧動作論理回路領域とを備え、

それぞれの前記電源端子は論理回路動作時に相互に電気的接続は無く、かつ前記保護素子の少なくとも１つは中央部、もしくはその近くに配置することを特徴とする半導体装置。

【請求項２】　半導体装置外から前記半導体装置内に電源を供給する第１の電源端子および第２の電源端子と、

前記半導体装置外から前記半導体装置内に電源を供給する第３の電源端子と第４の電源端子と第５の電源端子と、

前記第１の電源端子および第２の電源端子の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域と、

前記第３の電源端子と前記第２の電源端子を電源として動作する第２の電源電圧動作論理回路領域と、

前記第４の電源端子と前記第２の電源端子を電源として動作する第３の電源電圧動作論理回路領域と、

前記第５の電源端子と前記第２の電源端子を電源として動作する第４の電源電圧動作論理回路領域とを備え、

前記第２の電源端子は前記第１の電源端子の電圧に比べ低い電圧を供給する電源端子であり、

前記第３の電源端子、前記第４の電源端子、および前記第５の電源端子の電位は前記第２の電源端子電圧より高く、それぞれの電源端子は論理回路動作時に相互に電気的接続は無く、

前記第１の電源端子と第２の電源端子間、前記第３の電源端子と第２の電源端子間、第４の電源端子と第２の電源端子間、第５の電源端子と第２の電源端子間は、それぞれ静電破壊電荷から保護する保護素子を介して接続され、

前記第１の電源端子、第３の電源端子、第４の電源端子、および第５の電源端子は、相互に各々の電源端子に対して静電破壊電荷から保護する保護素子を介して接続され、

前記保護素子の少なくとも１つは中央部、もしくはその近くに配置することを特徴とする半導体装置。

【請求項３】　半導体装置外から前記半導体装置内に電源を供給する複数の電源端子と、

前記電源端子が複数組の対になり、各対における電源端子を電源として動作する半導体素子により構成される複数の電源電圧動作論理回路領域と、

前記各対における電源端子間に介在されてそれぞれ静電破壊電荷から保護する複数の保護素子とを備え、

それぞれの前記電源端子は論理回路動作時に相互に電気的接続は無く、かつ前記保護素子の少なくとも１つは中央部、もしくはその近くに配置することを特徴とする半導体装置。

【請求項４】　半導体装置外から前記半導体装置内に電源を供給する第１の電源端子および第２の電源端子と、

前記半導体装置外から前記半導体装置内に電源を供給する第３の電源端子、第４の電源端子、第５の電源端子、第６の電源端子、第７の電源端子、第８の電源端子と、

前記第１の電源端子および前記第２の電源端子の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域と、

前記第３の電源端子と前記第６の電源端子を電源として動作する第２の電源電圧動作論理回路領域と、

前記第４の電源端子と前記第７の電源端子を電源として動作する第３の電源電圧動作論理回路領域と、

前記第５の電源端子と前記第８の電源端子を電源として動作する第４の電源電圧動作論理回路領域とを備え、

前記第２の電源端子は第１の電源端子の電圧に比べ低い電圧を供給する電源端子であり、

前記第３の電源端子、第４の電源端子、第５の電源端子、第６の電源端子、第７の電源端子、および第８の電源端子のそれぞれの電源端子は回路動作時に相互に電気的接続は無く、

前記第１の電源端子と前記第２の電源端子、前記第３の電源端子と前記第６の電源端子、前記第４の電源端子と前記第７の電源端子、および前記第５の電源端子と第８の電源端子は、それぞれ静電破壊電荷から保護する保護素子を介して接続され、

前記第１電源電圧動作回路領域、前記第２電源電圧動作回路領域、前記第３電源電圧動作回路領域および前記第４電源電圧動作回路領域の電源端子間を相互接続する保護素子の少なくとも１つが、中央部もしくはその近くに配置することを特徴とする半導体装置。

【請求項５】　半導体装置外から前記半導体装置内に電源を供給する複数の電源端子と、

前記電源端子のうち低い電圧を供給する電源端子と他の電源端子との間に介在されてそれぞれ静電破壊電荷から半導体装置を保護する複数の保護素子と、

前記他の電源端子および前記低い電圧を供給する電源端子の電圧によってそれぞれ動作する半導体素子により構成される複数の電源電圧動作論理回路領域とを備え、

それぞれの前記電源端子は論理回路動作時に相互に電気的接続は無く、かつ前記保護素子の少なくとも１つは半導体装置の中央部、もしくはその近くに配置することを特徴とする半導体装置。

【請求項６】　半導体装置外から半導体装置内に電源を供給する第１の電源端子と第２の電源端子と、
半導体装置外から半導体装置内に電源を供給する第３の電源端子と第４の電源端子と第５の電源端子と、
前記第１の電源端子および前記第２の電源端子の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域と、
前記第３の電源端子と前記第２の電源端子を電源として動作する第２の電源電圧動作論理回路領域と、
前記第４の電源端子と前記第２の電源端子を電源として動作する第３の電源電圧動作論理回路領域と、
前記第５の電源端子と前記第２の電源端子を電源として動作する第４の電源電圧動作論理回路領域とを備え、
前記第２の電源端子は第１の電源端子の電圧に比べ低い電圧を供給する電源端子であり、
前記第３の電源端子、前記第４の電源端子、および前記第５の電源端子の電位は前記第２の電源端子電圧より高く、それぞれの電源端子は回路動作時に相互に電気的接続は無く、
前記第２の電源端子に対して、前記第１の電源端子、前記第３の電源端子、前記第４の電源端子、前記第５の電源端子が静電破壊電荷から保護する保護素子を介して相互接続し、前記保護素子の少なくとも１つは中央部、もしくはその近くに配置することを特徴とする半導体装置。
【請求項７】　保護素子は、回路動作時に漏れ電流以上の電流を流さないダイオード素子もしくはMOS 型トランジスタ素子またはバイポーラ型トランジスタ素子から構成された請求項１、請求項２、請求項３、請求項４、請求項５または請求項６記載の半導体装置。
【請求項８】　保護素子は、前記各々電源電圧動作論理回路領域への電源供給配線下に形成された請求項１、請求項２、請求項３、請求項４、請求項５、請求項６または請求項７記載の半導体装置。
【請求項９】　第１導電型の半導体基板と、この半導体基板上に形成して前記第１導電型の半導体基板と反対導電型であって前記半導体基板表面に対して多角形の形状で構成した第１の高濃度拡散領域と、この多角形の第１の高濃度拡散領域の辺と対向して静電破壊電荷保護素子として機能する一定距離の素子分離領域を挿入配置し前記第１の高濃度拡散領域と同導電型で多角形の形状を持つ第２の高濃度拡散領域とを備え、前記第１の高濃度拡散領域の各辺は前記第２の高濃度拡散領域と同型の拡散領域と対向することにより多角形の辺と同等数の保護素子を設け、各辺に形成される前記保護素子は異なる電源系統間の静電破壊電荷の通電経路となる接続としたことを特徴とする半導体装置。
【請求項１０】　複数の電圧耐圧を有する複数のMOS型トランジスタ素子を有し、異なる電源電圧系統により動作している複数の回路領域が存在し、前記複数の回路領域に対して、少なくとも１系統の電源電圧動作論理回路に対しての静電破壊保護素子が前記複数のMOS型トランジスタ素子の内、低電圧耐圧のMOS型トランジスタ素子により構成することを特徴とする半導体装置。
【請求項１１】　保護素子が複数種類の電圧耐圧MOS型トランジスタ素子を備えた請求項１、請求項２、請求項３、請求項４、請求項５、請求項６、請求項７、請求項８、請求項９または請求項１０記載の半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、少なくとも３つの電源系統を持つ多電源系統を有する半導体装置に於ける静電破壊を防止する保護形態を有する半導体装置に関するものである。また、半導体装置の微細化による半導体素子の低電圧耐圧化と、半導体装置を接続する周辺回路の高い電圧信号に対処する為に設ける高耐圧半導体素子を有効に用いた静電破壊防止形態を有する半導体装置に関するものである。
【０００２】
【従来の技術】従来、複数の電源系統を有する半導体装置、特に半導体論理回路における静電破壊防止回路技術としては、特公平６－５７０５号，特開平７－１０６４５５号，特開平８－３２１５８６号，特開平８－３１６４１８号，特開平９－１３９４６６号，特開平１０－５０９３２号が存在する。各公報にて開示された技術のポイントは以下の２つである。
（１）各電源系統間には静電破壊電荷を通電し、接地点までの経路を確保する保護素子を設ける。（通電経路に直列に並ぶ保護素子の段数、配線の寄生抵抗等は問かない（特開平７－１０６４５５号，特開平８－３１６４１８号，特開平９－１３９４６６号）。
（２）複数電源系統に対して共通の放電線を設けることを特徴として、静電破壊電荷を通電し、接地点までの経路上の保護素子数を２つとした静電破壊保護形態である（特開平８－３２１５８６号，特開平１０－５０９３２号）。
【０００３】それぞれの技術を以下説明する。まず、従来例（１）の技術であるが、図１１に示すＬＳＩの回路構成を用いて説明する。図１１では、ＶＳＳ電源はＶＳＳ１、ＶＳＳ２、ＶＳＳ３、ＶＳＳ４の４系統があり、ＶＤＤ電源はＶＤＤ１，ＶＤＤ２，ＶＤＤ３，ＶＤＤ４の４系統がある。Ｃ１で示したチップエリア内で、Ｉ１で示す論理回路エリア外はＬＳＩ周辺のエリアを示している。ここで、仮にＶＤＤ１を接地しＶＤＤ３に正の静電破壊電荷が印加されたとすると、正電荷は接地端に向かっていく。このとき通電経路の１つはＶＤＤ３からＧ２３の保護素子を通過してＶＤＤ２の配線を通り、さらにＧ２２の保護素子を通過してＶＤＤ１の接地端子へ流れる。もう一つの通電経路としてはＶＤＤ３からＧ１１の保護素子を通過してＶＳＳ１の配線を通り、さらにＧ

1の保護素子を介してVDD1の接地端子へ到達する。どちらの経路を通電するかは保護素子の特性と配線経路の抵抗成分、容量成分により決定する。本例では、2つの保護素子を通電して静電破壊電荷を逃がす場合を示したが、同様に複数の電源系を有するLSIではより多くの保護素子を通電して静電破壊電荷を逃がすことになる。

【0004】次に従来例（2）の回路技術であるが、図12にLSI回路構成例を提示する。図11の方式に新たに共通の放電用の配線である放電線LA1をチップエリア周辺の外部端子の外に設け、外部端子と放電線LA1間には保護素子G40を設けたものである。この方式では、静電破壊電荷は共通の放電線LA1を介して電荷を逃がすことを考えており、いくつ電源系が存在し、どの端子に静電破壊電荷を印加しても最大2つの保護素子のみを介して電荷を逃がすことが可能となる。

【0005】一方、静電破壊保護素子の素子形状に関してであるが、CMOSプロセスでは基本的には図5に示したN＋拡散領域n1，P－型ウエルp2，N＋拡散領域n2，およびP＋拡散領域p1で構成されるNPNバイポーラ構成、もしくは図6で示したN＋拡散領域n1、N＋拡散領域n2およびゲートGa1で構成されるNch型MOSトランジスタ構成となる。無論、拡散領域，ウエルの極性を逆にしたPNPバイポーラ構成，Pch型MOSトランジスタ構成も場合により使用する。これらの回路をデバイスレイアウトパターンとした場合には、一般的に知られた図7、図8（A）の梯形構成がある。また、トランジスタのゲート電極（もしくは拡散領域の分離エリア）をメッシュ状にしたメッシュゲート保護素子、さらに多角形や円形のゲート構成とした保護素子形状が提案されている。

【0006】一方、保護素子の静電破壊電荷を逃がす際の特性を改善し、保護素子面積を小さくする為に、製造工程の追加やマスクパターンの追加が行なわれている。

【0007】

【発明が解決しようとする課題】本発明が解決する課題は、複数の電源系を1デバイス上に有するLSIに於て、静電破壊電荷からのデバイス保護を面積増加を最小限にとどめて行なうものである。

【0008】まず、最初に保護素子の説明をして、その後課題の詳細を示す。保護素子の形状は既に述べたように図5、図6で示したバイポーラ型トランジスタもしくはMOS型トランジスタで構成される。LSIが通常の動作を行なっている場合には図5のバイポーラ型トランジスタではベース端子となる基板とコレクタ端子が接続され、エミッタ端子とベース端子により構成されるN＋とP－の半導体ジャンクションの逆バイアス耐圧は絶対最大定格以上の電圧となっている為に漏れ電流以上の電流は発生しない。一方、MOS型トランジスタの場合、ゲート電極はトランジスタのソースと接続されている為にLSIが通常の動作を行なっている場合には常にオフしている。MOS型トランジスタで構成した場合の保護素子の静電破壊電荷印加時の動作はバイポーラトランジスタと同様となる。静電破壊電荷は正極性、負極性のいずれかを持ち、また帯電物や放電経路に拠って電位や電荷量、そして時間軸上の過渡特性が異なってくる。保護素子の動作を説明する上で正電荷と負電荷の静電破壊について示す。

【0009】図6のMOS型トランジスタのドレインD1に正極性を持つ静電破壊電荷が印加された場合の特性を図10の特性グラフに示す。N＋の拡散領域D1とP－基板p2で構成されるダイオードは逆バイアスとなり、ドレインD1とソースS1（基板電位）の電位差が一定の電位に達し時にアバランシェブレークダウンを生じ、ドレインから基板、そしてソースへ電流を流しはじめる。このとき、ドレインD1とソースS1の電位差はアバランシェブレークダウンを生じた電位より低電圧ではほ固定される。さらに、ドレインD1電位を上げると図10の特性グラフで示した2次降伏電流、2次降伏電圧の時点で保護素子自体の破壊が生じる。図10で示した保護素子の特性はスナップバック特性とも言われるものであり、近年の微細プロセスでは、10V～15V程度でアバランシェブレイクダウン電位となり、2次降伏電圧、電流は2～3V前後で単位ゲート幅当たり、数十mA／μm 程度となる。一方、MOS型トランジスタのドレインD1に負極性を持つ静電破壊電荷が印加された場合には、N＋拡散領域D1とP－基板p2のダイオードは順方向バイアスとなり、ダイオードの両端子間の電位差が約0．7V 程度で電流を流しはじめ、電位はほぼ一定に固定される。一般的に順方向バイアスの方が流せる電流量が多い。

【0010】以上の保護素子特性に加えて、外部端子から保護素子までの配線の寄生素子成分とその他の通常回路迄の配線の寄生素子成分を考慮することが重要である。静電破壊電荷による電流量は一般的に数A流れるが、寄生抵抗成分による電位の上昇と保護素子が通電した際の固定電位の和により通電経路の電位が決定され、この電位が半導体素子の耐圧を超えない値とすることが必要である。また、保護素子が電流を流し始める迄のタイミングに対して、他の半導体素子に電位がかからない様に電位上昇を遅延させる為に容量成分を場合により付加させる事も考えられる。以上の静電破壊電荷から半導体素子を保護する形態に対して本発明では主として下記の3点に関して解決するものである。

【0011】従来の技術の中で説明した従来例（1）の各電源系統間に静電破壊電荷を通電し、接地点までの経路を確保する保護形態の課題を図11を用いて説明する。まず仮に、VDD3を接地点としてOUT1に静電破壊電荷を印加したとすると、保護素子G2、保護素子G21、保護素子G24を経てVDD3端子まで電荷は

到達する。保護素子の通電した際の固定電圧を2Vとすると3素子直列になっている為に6Vの電位差を生じている。通電する経路の寄生抵抗はシート抵抗0．1Ω／□、配線長を20mm（10mm□の半導体装置，対向する端子と仮定），配線幅を100μm，とすると20Ω程度となる。

【0012】静電破壊電荷による電流を1Aとすると配線寄生抵抗では20Vの電位が発生する。保護素子と配線寄生抵抗による電位は合計26V となる。ここで、静電破壊電荷が負極性を持っていたとすると、内部回路（論理回路領域L1）のPchトランジスタL1P1の基板と拡散領域により形成されるダイオードL1P1D1が順方向電位により0．7Vの電位差だけで電流を流す事から、論理回路領域L3のPchトランジスタL3P1のゲート電圧に16V以上の電位がかかることが想定できる。近年の微細プロセスに於けるMOS トランジスタの瞬時ゲート耐圧が16V程度とするとPchトランジスタのゲート破壊が生じる事は容易に考えられる。

【0013】さらに複数電源系統を想定すると保護素子は直列に複数個つながり、より電位差が発生することが懸念される。

【0014】一方、従来の技術の中で説明した従来例（2）に関して、図12を使用して詳細を説明する。図12の場合では、静電破壊電荷を逃がす経路の保護素子の段数を削減したものである。その為に別途共通の放電線LA1を設けていることが最大の特徴といえる。いくつ電源系統が増加しても、最大2つの保護素子が直列に接続されるのみであるため、保護素子による電圧の上昇が上述の例で4Vのみである。ただし、この方式でも静電破壊電荷を逃がす経路上の放電線の寄生抵抗を減らすことは出来ず、また別途配線を設けることによりレイアウト面積の増加は否めない。

【0015】保護素子レイアウトとしては、図5のバイポーラ型トランジスタと図6のMOS型トランジスタのいずれかの形状をもつ、図7、図8（A）の梅形レイアウト形状とメッシュ型レイアウトがある。n1～n8はN＋半導体拡散領域、p1～p3はP＋半導体拡散領域、E1はバイポーラ型トランジスタエミッタ端子、C1はバイポーラ型トランジスタコレクタ端子、D1はMOS型トランジスタドレイン端子、S1はMOS型トランジスタソース端子、Ga1,Ga2 はMOS型トランジスタゲート端子、r1は基板抵抗、r2は保護素子近傍、保護素子以外の半導体素子禁止領域、v1，v2は拡散領域―アルミ配線コンタクト素子、vp1はゲート電極―アルミ配線コンタクト素子である。

【0016】梅形レイアウト形状は従来より使用されているレイアウトであり、メッシュ型は比較的新しいレイアウト手法であるが、いずれも2系統の電位系間の保護素子である。ここで、図8（A）を使い5電源系間の保護素子レイアウト面積を計算する。対向する拡散領域の辺の幅を200μm、対向する拡散領域の間隔を0．5μm、5系統の電源間相互に保護素子を形成する場合に梅形保護素子では図8（A）の形状となる。保護素子の拡散領域の他の拡散領域とは対向しない辺の幅を10μmとすると図8（A）の保護素子レイアウト面積は横方向に115μm、縦方向に200μmとなり、総面積は23000μm^2 となる。

【0017】本発明は、記述の課題を解決し、かつ容易に実施出来る形態の半導体装置を提案するものである。

【0018】したがって、この発明の第1の目的は、多電源系統を有するLSIに於て、如何なる静電破壊電荷も保護素子を直列に3段以下の接続とすること、電源間の保護素子をLSI中心部、もしくはその周辺に配置することで静電破壊電荷の通電経路の寄生抵抗成分を削減することが可能となる半導体装置を提供することである。

【0019】第2の目的は、多電源系統を有するLSIで1系統でも共通電源が存在した場合には、共通の電源配線をターミナルノードとして保護素子を介した静電破壊電荷の通電経路を確保し、このとき保護素子が直列となる段数は例えば4段迄することができ、保護素子総数を削減出来る半導体装置を提供することである。

【0020】第3の目的は、保護素子の形状を多角形とし、各辺の保護素子の接続を別電源系とすることによる保護素子面積の削減を可能とする半導体装置を提供することである。

【0021】第4の目的は、近年の微細化による半導体素子の動作電源電圧の低下に対して半導体装置周辺の信号電圧が変化しないことにより、半導体装置上に2つの電圧耐圧を持つことが一般化されてきていることを有効に利用して、低電圧耐圧、低電圧クランプ素子による静電気電荷をスムースに接地端子に逃がすことができる半導体装置を提供することである。

【0022】

【課題を解決するための手段】請求項1記載の半導体装置は、半導体装置外から半導体装置内に電源を供給する複数の電源端子と、電源端子のうち低い電圧を供給する電源端子と他の電源端子との間に介在されてそれぞれ静電破壊電荷から半導体装置を保護する複数の第1の保護素子と、低い電圧を供給する電源端子の相互間に介在されて各々の電源端子に対して静電破壊電荷から保護する複数の第2の保護素子と、他の電源端子および低い電圧を供給する電源端子の電圧によってそれぞれ動作する半導体素子により構成される複数の電源電圧動作論理回路領域とを備え、それぞれの電源端子は論理回路動作時に相互に電気的接続は無く、かつ保護素子の少なくとも1つは中央部、もしくはその近くに配置することを特徴とするものである。

【0023】請求項1記載の半導体装置によれば、保護素子の段数を制限し、また実際の回路内への電源配線を

有効に使用して保護素子を配置することにより静電気による電荷の印加を接地端子へ逃がす経路を確保することができる。

【００２４】請求項２記載の半導体装置は、半導体装置外から半導体装置内に電源を供給する第１の電源端子および第２の電源端子と、半導体装置外から半導体装置内に電源を供給する第３の電源端子と第４の電源端子と第５の電源端子と、第１の電源端子および第２の電源端子の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域と、第３の電源端子と第２の電源端子を電源として動作する第２の電源電圧動作論理回路領域と、第４の電源端子と第２の電源端子を電源として動作する第３の電源電圧動作論理回路領域と、第５の電源端子と第２の電源端子を電源として動作する第４の電源電圧動作論理回路領域とを備え、第２の電源端子は第１の電源端子の電圧に比べ低い電圧を供給する電源端子であり、第３の電源端子、第４の電源端子、および第５の電源端子の電位は第２の電源端子電圧より高く、それぞれの電源端子は論理回路動作時に相互に電気的接続は無く、第１の電源端子と第２の電源端子間、第３の電源端子と第２の電源端子間、第４の電源端子と第２の電源端子間、第５の電源端子と第２の電源端子間は、それぞれ静電破壊電荷から保護する保護素子を介して接続され、第１の電源端子、第３の電源端子、第４の電源端子、および第５の電源端子は、相互に各々の電源端子に対して静電破壊電荷から保護する保護素子を介して接続され、保護素子の少なくとも１つは中央部、もしくはその近くに配置することを特徴とするものである。

【００２５】請求項２記載の半導体装置によれば、請求項１と同様な効果がある。

【００２６】請求項３記載の半導体装置は、半導体装置外から半導体装置内に電源を供給する複数の電源端子と、電源端子が複数組の対になり、各対における電源端子を電源として動作する半導体素子により構成される複数の電源電圧動作論理回路領域と、各対における電源端子間に介在されてそれぞれ静電破壊電荷から保護する複数の保護素子とを備え、それぞれの電源端子は論理回路動作時に相互に電気的接続は無く、かつ保護素子の少なくとも１つは中央部、もしくはその近くに配置することを特徴とするものである。

【００２７】請求項３記載の半導体装置によれば、請求項１と同様な効果がある。

【００２８】請求項４記載の半導体装置は、半導体装置外から半導体装置内に電源を供給する第１の電源端子および第２の電源端子と、半導体装置外から半導体装置内に電源を供給する第３の電源端子、第４の電源端子、第５の電源端子、第６の電源端子、第７の電源端子、第８の電源端子と、第１の電源端子および第２の電源端子の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域と、第３の電源端子と第６の電源端子を電源として動作する第２の電源電圧動作論理回路領域と、第４の電源端子と第７の電源端子を電源として動作する第３の電源電圧動作論理回路領域と、第５の電源端子と第８の電源端子を電源として動作する第４の電源電圧動作論理回路領域とを備え、第２の電源端子は第１の電源端子の電圧に比べ低い電圧を供給する電源端子であり、第３の電源端子、第４の電源端子、第５の電源端子、第６の電源端子、第７の電源端子、および第８の電源端子のそれぞれの電源端子は回路動作時に相互に電気的接続は無く、第１の電源端子と第２の電源端子、第３の電源端子と第６の電源端子、第４の電源端子と第７の電源端子、および第５の電源端子と第８の電源端子は、それぞれ静電破壊電荷から保護する保護素子を介して接続され、第１電源電圧動作回路領域、第２電源電圧動作回路領域、第３電源電圧動作回路領域および第４電源電圧動作回路領域の電源端子間を相互接続する保護素子の少なくとも１つが、中央部もしくはその近くに配置することを特徴とするものである。

【００２９】請求項４記載の半導体装置によれば、請求項１と同様な効果がある。

【００３０】請求項５記載の半導体装置は、半導体装置外から半導体装置内に電源を供給する複数の電源端子と、電源端子のうち低い電圧を供給する電源端子と他の電源端子との間に介在されてそれぞれ静電破壊電荷から半導体装置を保護する複数の保護素子と、他の電源端子および低い電圧を供給する電源端子の電圧によってそれぞれ動作する半導体素子により構成される複数の電源電圧動作論理回路領域とを備え、それぞれの電源端子は論理回路動作時に相互に電気的接続は無く、かつ保護素子の少なくとも１つは中央部、もしくはその近くに配置することを特徴とするものである。

【００３１】請求項５記載の半導体装置によれば、半導体装置内の多数の電源系の内、いずれかの電源系１系統を共有した論理回路構成であった場合、請求項１の効果に加えて保護素子数を削減することが可能である。

【００３２】請求項６記載の半導体装置は、半導体装置外から半導体装置内に電源を供給する第１の電源端子と第２の電源端子と、半導体装置外から半導体装置内に電源を供給する第３の電源端子と第４の電源端子と第５の電源端子と、第１の電源端子および第２の電源端子の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域と、第３の電源端子と第２の電源端子を電源として動作する第２の電源電圧動作論理回路領域と、第４の電源端子と第２の電源端子を電源として動作する第３の電源電圧動作論理回路領域と、第５の電源端子と第２の電源端子を電源として動作する第４の電源電圧動作論理回路領域とを備え、第２の電源端子は第１の電源端子の電圧に比べ低い電圧を供給する電源端子であり、第３の電源端子、第４の電源端子、および第５の電源端子の電位は第２の電源端子電圧より高く、

それぞれの電源端子は回路動作時に相互に電気的接続は無く、第２の電源端子に対して、第１の電源端子、第３の電源端子、第４の電源端子、第５の電源端子が静電破壊電荷から保護する保護素子を介して相互接続し、保護素子の少なくとも１つは半導体装置の中央部、もしくはその近くに配置することを特徴とするものである。

【００３３】請求項６記載の半導体装置によれば、請求項５と同様な効果がある。

【００３４】請求項７記載の半導体装置は、請求項１、請求項２、請求項３、請求項４、請求項５または請求項６において、保護素子が、回路動作時に漏れ電流以上の電流を流さないダイオード素子もしくはMIS 型トランジスタ素子またはバイポーラ型トランジスタ素子から構成されたものである。

【００３５】請求項７記載の半導体装置によれば、請求項１、請求項２、請求項３、請求項４、請求項５または請求項６と同様な効果がある。

【００３６】請求項８記載の半導体装置は、請求項１、請求項２、請求項３、請求項４、請求項５、請求項６または請求項７において、保護素子が、各々電源電圧動作論理回路領域への電源供給配線下に形成されたものである。

【００３７】請求項８記載の半導体装置によれば、請求項１、請求項２、請求項３、請求項４、請求項５、請求項６または請求項７と同様な効果がある。

【００３８】請求項９記載の半導体装置は、第１導電型の半導体基板と、この半導体基板上に形成して第１導電型の半導体基板と反対導電型であって半導体基板表面に対して多角形の形状で構成した第１の高濃度拡散領域と、この多角形の第１の高濃度拡散領域の辺と対向して静電破壊電荷保護素子として機能する一定距離の素子分離領域を挿入配置し第１の高濃度拡散領域と同導電型で多角形の形状を持つ第２の高濃度拡散領域とを備え、第１の高濃度拡散領域の各辺は第２の高濃度拡散領域と同型の拡散領域と対向することにより多角形の辺と同等数の保護素子を設け、各辺に形成される保護素子は異なる電源系統間の静電破壊電荷の逆電経路となる接続としたことを特徴とするものである。

【００３９】請求項９記載の半導体装置によれば、多電源系保護素子の素子形状を多角形のメッシュ構成とすることで更に面積を削減することが可能となる。

【００４０】請求項１０記載の半導体装置は、複数の電圧耐圧を有する複数のMOS型トランジスタ素子を有し、異なる電源電圧系統により動作している複数の回路領域が存在し、複数の回路領域に対して、少なくとも１系統の電源電圧動作論理回路に対しての静電破壊保護素子が複数のMOS型トランジスタ素子の内、低電圧耐圧のMOS型トランジスタ素子により構成することを特徴とするものである。

【００４１】請求項１０記載の半導体装置によれば、近年の微細化による半導体素子の動作電源電圧の低下に対して半導体装置周辺の信号電圧が変化しないことにより、半導体装置上に２つの電圧耐圧を持つことが一般化されてきていることを有効に利用して、保護素子に通電する際の電位差を低下させることが可能であり、静電気電荷印加端子から接地端子までの電位差上昇を下げることができる。

【００４２】請求項１１記載の半導体装置は、請求項１、請求項２、請求項３、請求項４、請求項５、請求項６、請求項７、請求項８、請求項９または請求項１０において、保護素子が複数種類の電圧耐圧MOS型トランジスタ素子を備えたものである。

【００４３】請求項１１記載の半導体装置によれば、請求項１、請求項２、請求項３、請求項４、請求項５、請求項６、請求項７、請求項８、請求項９または請求項１０と同様な効果がある。

【００４４】

【発明の実施の形態】従来技術の課題に対して、前記の課題解決する手段を用いた技術の実施形態を以下に示す。

【００４５】（実施の形態１）本発明の請求項１～４に対応する第１の実施の形態を図１、および図２を用いて説明する。図１、図２はそれぞれLSIのチップを模式的に示したものである。これらの図において、VDD１～VDD４、VSS１～VSS４は電源系統、IN１～IN４は信号入力端子、OUT１～OUT４は信号出力端子、IO－P１～IO－P８、IO－N１～IO－N８は入力信号、出力信号回路を構成する素子、G１～G３６は静電破壊保護素子、L１～L４は各電源系より電源を供給される論理回路領域、C１１は半導体装置枠、I１１は内部論理回路領域である。

【００４６】C１で示したLSIチップ内とI１で示す論理回路部分を持ち、チップ周辺に外部信号の入力／出力端子、または電源供給端子を設けている（本発明では端子をLSI外部に設けることに関しては得に規定はしていない）。各端子には言うまでもなくトランジスタ等半導体素子が接続されるが、それと共に半導体素子を外部の静電気などの過大な電荷から保護する保護素子が設けられる。半導体素子はIO－P１、IO－P２．．．．IO－P８，IO－N１、IO－N２．．．．IO－N８で示されるものである。接続される保護素子はG１、G２、G３．．．．G３６で示すものである。保護素子の機能は既に従来の技術の項で示したものである。本発明において特徴となるのは図１中の保護素子G２５、G２６をLSIのチップ内部I１１の論理回路部分に設けることにある。従来の技術で既述した図１１の形態では、既に述べたように複数系統の電源系を持つ場合において、直列に複数の保護素子を設け、また大きな寄生抵抗付けることは静電破壊電荷を通電させる際に一部半導体素子に過大な電荷を与えることが考

えられることは既に述べた。例として図１１を用い、またＶＤＤ３を接地点としてＯＵＴ１に静電破壊電荷を印加した場合を説明した。同じ条件で、図１の構成を用いた場合について示す。ＶＤＤ３を接地し、ＯＵＴ１に静電破壊電荷を印可した場合には電荷は保護素子Ｇ４、Ｇ２５を通電してＶＤＤ３に到達する。このとき直列に接続された保護素子により生じる電位は合計４Ｖ である。また、チップ内部Ｉ１の論理回路部分に保護素子を設けていることから配線長が短くなる。前記例と同等のチップサイズとすると１０ｍｍの配線長程度と考えられる。また、ＬＳＩ内部のＬＳＩの電源幹線の配線幅を１００μｍ とし、電源配線に重なり保護素子を形成すると寄生抵抗は１０Ωである。静電破壊電荷を通電させる経路に１Ａの電流が生じたとすると電荷印加端子の接地端子に対する電位差は１４Ｖである。隣接する電源系の保護素子は保護素子Ｇ２１、Ｇ２２、Ｇ２３、Ｇ２４の様に隣接する領域に配置するよう良いが、隣接しない電源系領域に対しては上述した様に素子のインピーダンスを下げることが重要である。

【００４７】図２に示した回路は図１の共通電源ＶＳＳ１を４系統のＶＳＳに分断した場合である。この場合も同様に、隣接しない異なる電源系に対してチップ内部Ｉ１の論理回路部分に保護素子Ｇ２５、Ｇ２６、Ｇ３１～Ｇ３６を設けていることで、１つは直列に接続される保護素子の個数を削減し、一方で配線寄生抵抗を削減している。

【００４８】このように、第１の実施の形態では図１において、半導体装置外から半導体装置内に電源を供給する第１の電源端子（ＶＤＤ１）および第２の電源端子（ＶＳＳ１）と、半導体装置外から半導体装置内に電源を供給する第３の電源端子（ＶＤＤ２）と第４の電源端子（ＶＤＤ３）と第５の電源端子（ＶＤＤ４）と、第１の電源端子（ＶＤＤ１）および第２の電源端子（ＶＳＳ１）の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域（Ｌ１）と、第３の電源端子（ＶＤＤ２）と第２の電源端子（ＶＳＳ１）を電源として動作する第２の電源電圧動作論理回路領域（Ｌ２）と、第４の電源端子（ＶＤＤ３）と第２の電源端子（ＶＳＳ１）を電源として動作する第３の電源電圧動作論理回路領域（Ｌ３）と、第５の電源端子（ＶＤＤ４）と第２の電源端子（ＶＳＳ１）を電源として動作する第４の電源電圧動作論理回路領域（Ｌ４）とを備え、第２の電源端子（ＶＳＳ１）は第１の電源端子（ＶＤＤ１）の電圧に比べ低い電圧を供給する電源端子であり、第３の電源端子（ＶＤＤ２）、第４の電源端子（ＶＤＤ３）、および第５の電源端子（ＶＤＤ４）の電位は第２の電源端子（ＶＳＳ１）電圧より高く、それぞれの電源端子は論理回路動作時に相互に電気的接続は無く、第１の電源端子（ＶＤＤ１）と第２の電源端子（ＶＳＳ１）間、第３の電源端子（ＶＤＤ２）と第２の電源端子（ＶＳＳ１）間、第４の電源端子（ＶＤＤ３）と第２の電源端子（ＶＳＳ１）間、第５の電源端子（ＶＤＤ４）と第２の電源端子（ＶＳＳ１）間は、それぞれ静電破壊電荷から保護する保護素子を介して接続され、第１の電源端子（ＶＤＤ１）、第３の電源端子（ＶＤＤ２）、第４の電源端子（ＶＤＤ３）、および第５の電源端子（ＶＤＤ４）は、相互に各々の電源端子に対して静電破壊電荷から保護する保護素子を介して接続され、保護素子の少なくとも１つは中央部、もしくはその近くに配置している。

【００４９】また、図２においては、半導体装置外から半導体装置内に電源を供給する第１の電源端子（ＶＤＤ１）および第２の電源端子（ＶＳＳ１）と、半導体装置外から半導体装置内に電源を供給する第３の電源端子（ＶＤＤ２）、第４の電源端子（ＶＤＤ３）、第５の電源端子（ＶＤＤ４）、第６の電源端子（ＶＳＳ２）、第７の電源端子（ＶＳＳ３）、第８の電源端子（ＶＳＳ４）と、第１の電源端子（ＶＤＤ１）および第２の電源端子（ＶＳＳ１）の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域（Ｌ１）と、第３の電源端子（ＶＤＤ２）と第６の電源端子（ＶＳＳ２）を電源として動作する第２の電源電圧動作論理回路領域（Ｌ２）と、第４の電源端子（ＶＤＤ３）と第７の電源端子（ＶＳＳ３）を電源として動作する第３の電源電圧動作論理回路領域（Ｌ３）と、第５の電源端子（ＶＤＤ４）と第８の電源端子（ＶＳＳ４）を電源として動作する第４の電源電圧動作論理回路領域（Ｌ４）とを備え、第２の電源端子（ＶＳＳ１）は第１の電源端子（ＶＤＤ１）の電圧に比べ低い電圧を供給する電源端子であり、第３の電源端子（ＶＤＤ２）、第４の電源端子（ＶＤＤ３）、第５の電源端子（ＶＤＤ４）、第６の電源端子（ＶＳＳ２）、第７の電源端子（ＶＳＳ３）、および第８の電源端子（ＶＳＳ４）のそれぞれの電源端子は回路動作時に相互に電気的接続は無く、第１の電源端子（ＶＤＤ１）と第２の電源端子（ＶＳＳ１）、第３の電源端子（ＶＤＤ２）と第６の電源端子（ＶＳＳ２）、第４の電源端子（ＶＤＤ３）と第７の電源端子（ＶＳＳ３）、および第５の電源端子（ＶＤＤ４）と第８の電源端子（ＶＳＳ４）は、それぞれ静電破壊電荷から保護する保護素子を介して接続され、第１電源電圧動作回路領域（Ｌ１）、第２電源電圧動作回路領域（Ｌ２）、第３電源電圧動作回路領域（Ｌ３）および第４電源電圧動作回路領域（Ｌ４）の電源端子間を相互接続する保護素子の少なくとも１つが、中央部もしくはその近くに配置している。

【００５０】（実施の形態２）本発明の請求項５、６に対応する、第１の実施の形態においてさらに電源系が増加した場合の第２の実施の形態を図４に示す。Ｇ３７、Ｇ３８は保護素子であり、その他は第１の実施の形態と同じである。

【００５１】まず、図３は隣接しない電源系に対しての保護素子の挿入形態を示している。チップ内部Ｉ１の論理回路部分に挿入した保護素子Ｇ３７が２０個存在している。既に第１の実施の形態で述べたように隣接しない電源系に対してチップ内部Ｉ１に保護素子を設けることは寄生抵抗成分を削減することと直列に接続する保護素子の段数を削減する上で効果的であり、静電破壊電荷より半導体素子を保護する場合に有効である。しかしながら電源系統の増加により保護素子が増加することでＬＳＩのチップ面積の増大が生じる。

【００５２】そこで、１系統でも共通の電源がある場合は、その共有電源をターミナルノードとして保護素子の数を減らした場合を図４に示す。図４ではＶＳＳ１を共有電源としている為に保護素子Ｇ３８の個数は８系統のみに削減されている。上記例の場合と同様にある電源端子を接地して、任意の端子に静電破壊電荷を印加したとする。上述の例では出力端子ＯＵＴ１に静電破壊電荷を印加した場合、保護素子を介してＶＤＤ１電源配線に電荷を通電し、ＶＤＤ３の接地端子の接地点まで保護素子を介して電荷を逃がしていた。第２の実施の形態の例として図４のＶＤＤ５を接地端子とした場合で、ＶＤＤ１の電源配線に電荷が通電され、１つの保護素子Ｇ３８に通電した後ＶＳＳ１配線を一旦介するが、さらにＶＤＤ５側の保護素子Ｇ３８を通電し、接地端ＶＤＤ５に電荷は逃げることになる。第２の実施の形態で示した発明に関して、通常共有電源配線は図１で示した様にチップＣ１の外周近傍に配線されるものであるが、チップ上、対向する電源系等における電源間保護を形成する際の寄生抵抗成分を削減できるものであり、また、共通電源の外部端子をＩ１で示したチップ内部に設け、直接電源を供給する際に静電破壊経路を形成する場合に有効である。

【００５３】このように、第２の実施の形態における半導体装置は、半導体装置外から半導体装置内に電源を供給する第１の電源端子（ＶＤＤ１）と第２の電源端子（ＶＳＳ１）を備え、第２の電源端子（ＶＳＳ１）は第１の電源端子（ＶＤＤ１）の電圧に比べ低い電圧を供給する電源端子であり、上記の２つの電源端子の電圧によって動作する半導体素子により構成される第１の電源電圧動作論理回路領域と、加えて半導体装置外から半導体装置内に電源を供給する第３の電源端子（ＶＤＤ２）と第４の電源端子（ＶＤＤ３）と第５の電源端子（ＶＤＤ４）と第６の電源端子（ＶＤＤ５）と第７の電源端子（ＶＤＤ６）と第８の電源端子（ＶＤＤ７）を備え、第３の電源端子（ＶＤＤ２）と第４の電源端子（ＶＤＤ３）と第５の電源端子（ＶＤＤ４）と第６の電源端子（ＶＤＤ５）と第７の電源端子（ＶＤＤ６）と第８の電源端子（ＶＤＤ７）の電位は第２の電源端子（ＶＳＳ１）電圧より高く、それぞれの電源端子は回路動作時に電気的接続は無く、第３の電源端子（ＶＤＤ２）と第２の電源端子（ＶＳＳ１）を電源として動作する第２の電源電圧動作論理回路領域と、第４の電源端子（ＶＤＤ３）と第２の電源端子（ＶＳＳ１）を電源として動作する第３の電源電圧動作論理回路領域と、第５の電源端子（ＶＤＤ４）と第２の電源端子（ＶＳＳ１）を電源として動作する第４の電源電圧動作論理回路領域と、第６の電源端子（ＶＤＤ５）と第２の電源端子（ＶＳＳ１）を電源として動作する第５の電源電圧動作論理回路領域と、第７の電源端子（ＶＤＤ６）と第２の電源端子（ＶＳＳ１）を電源として動作する第６の電源電圧動作論理回路領域と、第８の電源端子（ＶＤＤ７）と第２の電源端子（ＶＳＳ１）を電源として動作する第７の電源電圧動作論理回路領域とを備え、第２の電源端子（ＶＳＳ１）に対して、第１の電源端子（ＶＤＤ１）、第３の電源端子（ＶＤＤ２）、第４の電源端子（ＶＤＤ３）、第５の電源端子（ＶＤＤ４）、第６の電源端子（ＶＤＤ５）、第７の電源端子（ＶＤＤ６）、第８の電源端子（ＶＤＤ７）が静電破壊電荷から半導体装置を保護する保護素子を介して相互接続し、保護素子の少なくとも１つは中央部、もしくはその近くに配置している。

【００５４】第２の実施の形態によれば、多電源系統を有するＬＳＩで１系統でも共通電源が存在した場合には、共通の電源配線をターミナルノードとして保護素子を介した静電破壊電荷の通電経路を確保し、異なる電源間で直列接続される保護素子段数は最大２段までとすることができ、保護素子総数を削減できる。ただし、段数は３段、４段あるいはそれ以上とすることが可能である。

【００５５】なお、保護素子は、例えば半導体装置の回路動作時に漏れ電流以上の電流を流さないダイオード素子もしくはＭＯＳ型トランジスタ素子またはバイポーラ型トランジスタ素子から構成される。また保護素子は、各々電源電圧動作論理回路領域への電源供給配線下に形成される。

【００５６】（実施の形態３）本発明の請求項９に対応する第３の実施の形態を図８および図９により説明する。請求項９の発明は多角形の拡散領域で構成される保護素子の各辺を１つの電源間保護素子として構成したものであり、例として図８（Ｂ）および図９に示す構成となる。図８（Ｂ）は５系統の電源間保護素子を形成したものであり、Ｇ３９で示す保護素子の領域を特に拡大したものが図９である。図８（Ｂ）で各ますめに入っているＡ，Ｂ，Ｃ，Ｄ，Ｅ，Ｆが電源系統を示すものであり、ますめの中は拡散領域である。拡散領域の各辺は対向する電源との間の保護素子となる。発明が解決しようとする課題で示した楕形の保護素子レイアウトの面積計算と同様に本発明の実施の形態を説明する。楕形の保護素子レイアウトでは２００μｍの幅で拡散領域が対向していた。多電源メッシュ型保護素子でも同様の拡散領域の対向幅とする条件で面積計算を行う。メッシュ内にあるますめの一辺を５μｍとすると図８（Ｂ）に示した様

にまするれば縦１２個、横２２個とすることで拡散領域対向幅２００μm 以上が確保される。対向する拡散領域の間隔を０．５μmとすると面積は７８９２．７５μm^2となる。前述の櫛形の保護素子レイアウトのレイアウト面積が２３０００μm と比較すると約３４．３%のレイアウト面積となり、非常に小面積となる。

【００５７】このように、第３の実施の形態では、第１導電型の半導体基板と、この半導体基板上に形成して第１導電型の半導体基板と反対導電型であって半導体基板表面に対して多角形の形状で構成した第１の高濃度拡散領域（Ａ）と、この多角形の第１の高濃度拡散領域（Ａ）の辺と対向して静電破壊電荷保護素子として機能する一定距離の素子分離領域を挿入配置し第１の高濃度拡散領域（Ａ）と同導電型で多角形の形状を持つ第２の高濃度拡散領域（Ｂ，Ｃ，Ｄ，Ｅ）とを備え、第１の高濃度拡散領域（Ａ）の各辺は第２の高濃度拡散領域（Ｂ，Ｃ，Ｄ，Ｅ）と同型の拡散領域と対向することにより多角形の辺と同等数の保護素子を設け、各辺に形成される保護素子は異なる電源系統間の静電破壊電荷の通電経路となる接続としている。

【００５８】これにより、多電源系保護素子の素子形状を多角形のメッシュ構成とすることで更に面積を削減することが可能となる。上記の多角形の角数は無限大となり、高濃度拡散領域が円形となる場合も含む。

【００５９】（実施の形態４）本発明の請求項１０に対応した第４の実施の形態を図１０を用いて説明する。図１０において、ＬＢ１，ＬＢ２はゲート実効長、Ga2 はＭＯＳ型トランジスタゲート端子、その他は他の図について説明したのと同様である。

【００６０】ＣＭＯＳ半導体装置の標準動作電源電圧が０．６μmプロセス世代まで５Ｖであったものが０．５μm プロセス世代で３．３Ｖとなり、０．２５μm プロセス世代以降で世代毎に標準動作電源電圧が低下することは周知の事実である。しかしながら、ＣＭＯＳ半導体装置の周辺装置は従来からの５Ｖ系信号や３．３Ｖ系信号が存在する。この為ＣＭＯＳ半導体装置内に異なる電圧耐圧のトランジスタを混載させることが考えられる。それぞれのトランジスタの構成に於いて異なる部分で顕著な部分はＭＯＳ型トランジスタでのゲート酸化膜厚とゲート長である。一方、ＣＭＯＳ半導体プロセスに於けるバイポーラ型トランジスタの構成は、ＭＯＳ型トランジスタのゲートを削除した形状となる。静電破壊保護トランジスタの動作はＭＯＳ型、バイポーラ型共にバイポーラ型トランジスタ動作をする。ここで、ＭＯＳ型で定義されているパラメータであるゲート長をバイポーラ型トランジスタのエミッタ、コレクタ間拡散領域間隔として使用する。ゲート長にたいしてのトランジスタのオン電圧依存性は "H.Weston,Y.Lee,T.Stanik, 'A Newly Observed High Frequency Effect on the ESD Protection Utilized in a Gigahertz NMOS Technology',in Proc. 14th EOS/ESD Symposium,P.95-98,1992" で示されている様にゲート長が短くなるほどオン電圧が低下する。図１０（Ａ）を５Ｖ耐圧トランジスタでゲート長ＬＢ１を０．６μm，図１０（Ｂ）を３．３ｖ耐圧トランジスタでゲート長ＬＢ２を０．４μm とすると、図１０（Ｃ）の用にＮＰＮトランジスタの電位は想像線Ｋ１、Ｋ３から実線Ｋ２、Ｋ４の特性へと変化する。前記資料では１／２程電位を低下させることが可能である。図１に於いて例えば、ＶＤＤ１とＶＤＤ３の電源電圧が３．３Ｖとするとゲ２５の保護素子を３．３Ｖ耐圧トランジスタにて構成することで保護素子を通電する際に発生させる電位差を低下させることが可能となる。

【００６１】このように、第４の実施の形態では、複数の電圧耐圧を有する複数のＭＯＳ型トランジスタ素子（図１０（Ａ），（Ｂ））を有し、異なる電源電圧系統により動作している複数の回路領域が存在し、複数の回路領域に対して、少なくとも１系統の電源電圧動作論理回路に対しての静電破壊保護素子が複数のＭＯＳ型トランジスタ素子（図１０（Ａ），（Ｂ））の内、低電圧耐圧のＭＯＳ型トランジスタ素子（図１０（Ｂ））により構成している。

【００６２】これにより、近年の微細化による半導体素子の動作電源電圧の低下にたいして半導体装置周辺の信号電圧のが変化しないことにより、半導体装置上に２つの電圧耐圧を持つことが一般化されてきていることを有効に利用して、保護素子の通電する際の電位差を低下させることが可能であり、静電気電荷印加端子から接地端子までの電位差上昇を下げることができる。

【００６３】なお、電源端子数は上記の各実施の形態に記載に限らずそれ以上でもよく、その際にも上記の接続関係を拡張して適応可能である。また保護素子は、半導体装置の回路動作時に漏れ電流以上の電流を流さないダイオード素子もしくはMOS 型トランジスタ素子またはバイポーラ型トランジスタ素子から構成されてもよい。また保護素子が各々電源電圧動作論理回路領域への電源供給配線下に形成されてもよい。さらに保護素子は２種類の電圧耐圧を有するＭＯＳ型トランジスタ素子に限らず、半導体装置において２種類以上の電圧耐圧ＭＯＳ型トランジスタ素子を用いたものでもよい。

【００６４】

【発明の効果】請求項１記載の半導体装置によれば、保護素子の段数を制限し、また実際の回路内への電源配線を有効に使用して保護素子を配置することにより静電気による電荷の印加を接地端子へ逃がす経路を確保することができる。

【００６５】請求項２記載の半導体装置によれば、請求項１と同様な効果がある。

【００６６】請求項３記載の半導体装置によれば、請求項１と同様な効果がある。

【００６７】請求項４記載の半導体装置によれば、請求

項１と同様な効果がある。

【００６８】請求項５記載の半導体装置によれば、半導体装置内の多数の電源系の内、いずれかの電源系１系統を共有した論理回路構成であった場合、請求項１の効果に加えて保護素子数を削減することが可能である。

【００６９】請求項６記載の半導体装置によれば、請求項５と同様な効果がある。

【００７０】請求項７記載の半導体装置によれば、請求項１、請求項２、請求項３、請求項４、請求項５または請求項６と同様な効果がある。

【００７１】請求項８記載の半導体装置によれば、請求項１、請求項２、請求項３、請求項４、請求項５、請求項６または請求項７と同様な効果がある。

【００７２】請求項９記載の半導体装置によれば、多電源系保護素子の素子形状を多角形のメッシュ構成とすることで更に面積を削減することが可能となる。

【００７３】請求項１０記載の半導体装置によれば、近年の微細化による半導体素子の動作電源電圧の低下に対して半導体装置周辺の信号電圧が変化しないことにより、半導体装置上に２つの電圧耐圧を持つことが一般化されてきていることを有効に利用して、保護素子に通電する際の電位差を低下させることが可能であり、静電気電荷印加端子から接地端子までの電位差上昇を下げることができる。

【００７４】請求項１１記載の半導体装置によれば、請求項１、請求項２、請求項３、請求項４、請求項５、請求項６、請求項７、請求項８、請求項９または請求項１０と同様な効果がある。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態を示す回路図である。

【図２】本発明の第１の実施の形態の変形形態を説明する回路図である。

【図３】本発明の第２の実施の形態の前提となる例を説明する説明図である。

【図４】本発明の第２の実施の形態を説明する回路図である。

【図５】バイポーラ型トランジスタ保護素子の形状を説明する概略断面図である。

【図６】ＭＯＳ型トランジスタ保護素子の形状を説明する概略断面図である。

【図７】バイポーラ型トランジスタ保護素子の櫛形構成レイアウトパターン図である。

【図８】（Ａ）はバイポーラ型トランジスタ保護素子の多電源系櫛形構成の第３の実施の形態の前提となるレイアウトパターン、（Ｂ）はバイポーラ型トランジスタ保護素子の多電源メッシュ構成レイアウトパターンであり、第３の実施の形態を説明する図である。

【図９】図８（Ｂ）のレイアウトの一部を切り出した拡大図である。

【図１０】第４の実施の形態を示し、（Ａ）はＭＯＳ型トランジスタ保護素子の内、ゲート長が長いトランジスタを示し、（Ｂ）はＭＯＳ型トランジスタ保護素子の内、ゲート長が短いトランジスタを示し、（Ｃ）はトランジスタ保護素子のスナップバック特性であり、ゲート長の差異による特性差を示したものである。

【図１１】従来例（１）を説明する回路図である。

【図１２】従来例（２）を説明する回路図である。

【符号の説明】

ＶＤＤ１，ＶＤＤ２，・・・ＶＤＤ７，ＶＳＳ１，ＶＳＳ２，ＶＳＳ３，ＶＳＳ４：電源系統

ＩＮ１，ＩＮ２，ＩＮ３，ＩＮ４：信号入力端子

ＯＵＴ１，ＯＵＴ２，ＯＵＴ３，ＯＵＴ４：信号出力端子

ＩＯ－Ｐ１，ＩＯ－Ｐ２，・・・ＩＯ－Ｐ８，ＩＯ－Ｎ１，ＩＯ－Ｎ２，・・・ＩＯ－Ｎ８：入力信号、出力信号回路を構成する素子

Ｇ１，Ｇ２，・・・Ｇ４０：静電破壊保護素子

Ｌ１，Ｌ２，Ｌ３，Ｌ４：各電源系より電源を供給される論理回路領域

Ｃ１：半導体装置枠

Ｉ１：内部論理回路領域

ｎ１，ｎ２，・・・ｎ９：Ｎ＋半導体拡散領域

ｐ１，ｐ２，ｐ３：Ｐ＋半導体拡散領域

Ｅ１：バイポーラ型トランジスタエミッタ端子

Ｃ１：バイポーラ型トランジスタコレクタ端子

Ｄ１：ＭＯＳ 型トランジスタドレイン端子

Ｓ１：ＭＯＳ型トランジスタソース端子

Ｇａ１，Ｇａ２：ＭＯＳ型トランジスタゲート端子

ｒ１：基板抵抗

ｒ２：保護素子近傍、保護素子以外の半導体素子禁止領域

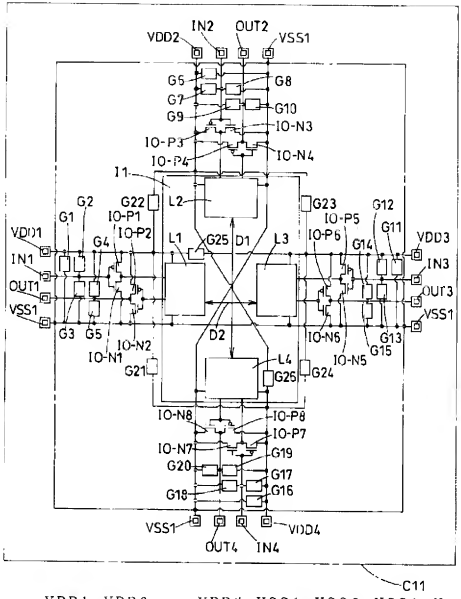
ｖ１，ｖ２：拡散領域－アルミ配線コンタクト素子

ｖｐ１：ゲート電極－アルミ配線コンタクト素子

Ａ，Ｂ，Ｃ，Ｄ，Ｅ：電源系統／高濃度拡散領域

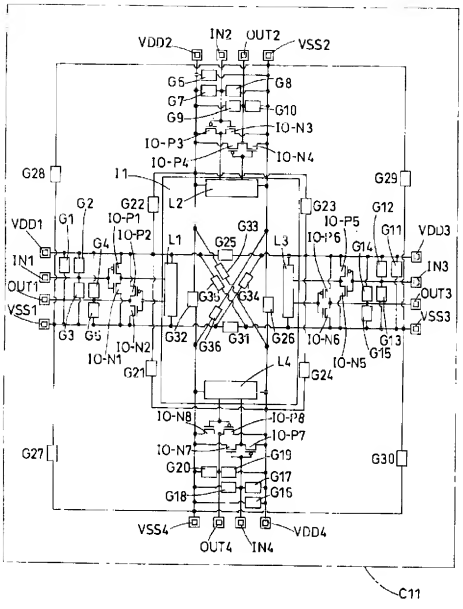
ＬＢ１，ＬＢ２：ゲート実効長

【図1】

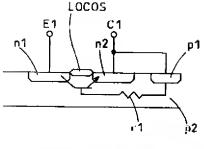


VDD1, VDD2, ・・・VDD7, VSS1, VSS2, VSS3, VSS4…電源系統
IN1, IN2, IN3, IN4…信号入力端子
OUT1, OUT2, OUT3, OUT4…信号出力端子
IO-P1, IO-P2, ・・・IO-P8, IO-N1, IO-N2, ・・・IO-N8…入力信号、出力信号回路を構成する素子
G1, G2, ・・・G38…静電破壊保護素子
L1, L2, L3, L4…各電源系より電源を供給される論理回路領域
C1…半導体装置枠

【図2】

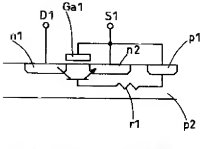


【図5】



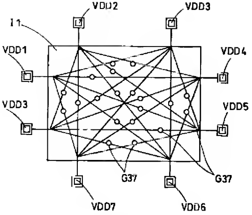
n1, n2, ・・・n9…N+半導体拡散領域
p1, p2, p3…P+半導体拡散領域
E1…バイポーラ型トランジスタエミッタ端子
C1…バイポーラ型トランジスタコレクタ端子

【図6】



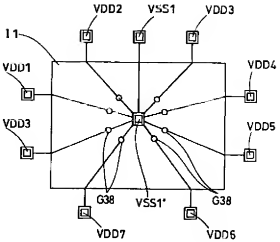
D1…MOS型トランジスタドレイン端子
S1…MOS型トランジスタソース端子

【図3】

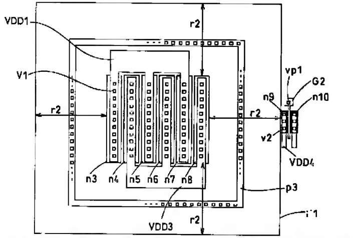


I1…内部論理回路領域

【図4】



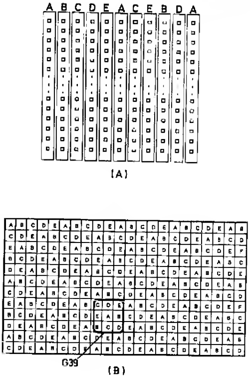
【図7】



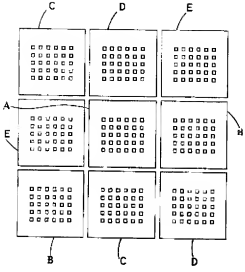
r1…基板抵抗
r2…保護素子近傍、保護素子以外の半導体素子禁止領域
v1, v2…拡散領域－アルミ配線コンタクト素子
vp1…ゲート電極－アルミ配線コンタクト素子

【図8】

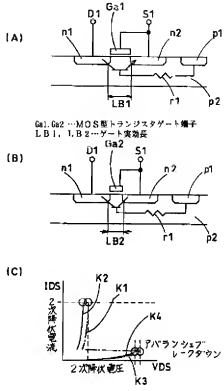
A, B, C, D, E…電源系統



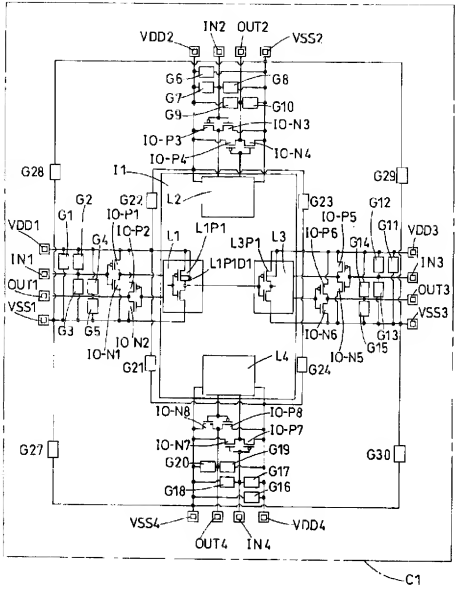
【図9】


C
D
E
A
E
H
B
C
D

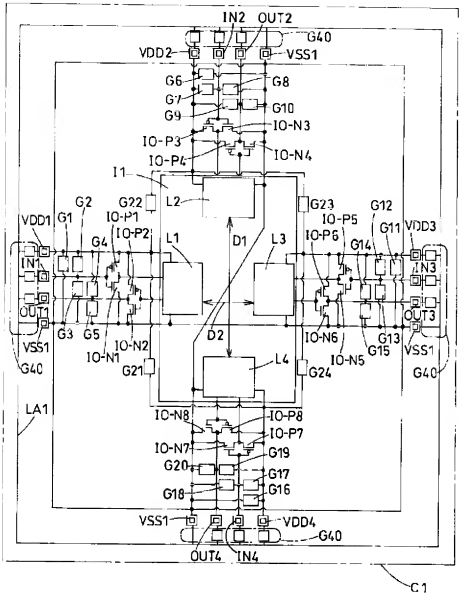
【図10】


(A)
D1
Ga1
S1
n1
n2
p1
LB1
r1
p2
Ga1, Ga2…MOS型トランジスタゲート端子
LB1, LB2…ゲート実効長
(B)
D1
Ga2
S1
n1
n2
p1
LB2
r1
p2
(C)
IDS
K2
K1
K4
K3
VDS
2次降伏電圧
1/アバランシェ・ブレークダウン

【図11】


VDD2
IN2
OUT2
VSS2
G6
G8
G7
G9
G10
IO-N3
IO-P3
IO-P4
IO-N4
G28
I1
G29
G2
G22
L2
G23
G12
G1
IO-P1
IO-P5
VDD1
IO-P2
L1
L1P1
L3P1
L3
IO-P6
G14
G11
VDD3
IN1
G4
L1P1D1
IN3
OUT1
OUT3
VSS1
VSS3
G3
G5
IO-N1
IO-N2
IO-N6
G13
G15
IO-N5
G21
L4
G24
IO-N8
IO-P8
IO-P7
G27
IO-N7
G19
G30
G20
G17
G18
G16
VSS4
VDD4
OUT4
IN4
C1

【図12】


IN2
OUT2
G40
VDD2
VSS1
G6
G8
G7
G10
G9
IO-N3
IO-P3
IO-N4
IO-P4
I1
G2
G22
L2
G23
G12
VDD1
G1
IO-P1
IO-P5
G11
VDD3
IO-P2
L1
D1
L3
IO-P6
G14
G4
IN1
IN3
OUT1
OUT3
G3
G5
D2
IO-N6
G13
VSS1
VSS1
IO-N2
IO-N1
IO-N5
G15
G40
G21
L4
G24
G40
LA1
IO-N8
IO-P8
IO-P7
IO-N7
G19
G20
G17
G18
G16
VSS1
VDD4
G40
OUT4
IN4
C1

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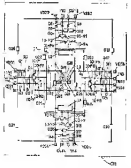
(21)Application number : 11-010704 (71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

(22)Date of filing : 19.01.1999 (72)Inventor : YAMAMOTO HIROO

(54) SEMICONDUCTOR DEVICE



(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the parasitic resistance component of the energizing route of electrostatic breakdown charges by not electrically connecting power supply terminals to each other when a logic circuit operates and, in addition, arranging, at least, one protective element in a central part or its

vicinity.

SOLUTION: A semiconductor device has a logic circuit section in an LSI chip, and input/output terminals for external signal or power supply terminals in the periphery of the chip. A semiconductor element is connected to each terminal and, in addition, a protective element which protects the semiconductor element from excessive charges, such as external static electricity, etc., is provided. The protective elements connected to the terminals are those G1, G2, G3,..., G36, of which G25 and G26 are provided in the logic circuit section provided in II the LSI chip. Since the protective elements are arranged by limiting the number of stages of the elements and effectively using the power supply wiring to an actual circuit, a route for relieving charges caused by static electricity and impressed upon the semiconductor elements to a grounding terminal can be secured.

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]

[Claim 1] Two or more power supply terminals which supply a power source in said semiconductor device from the outside of a semiconductor device, Two or more 1st protection components which intervene between the power supply terminal which supplies a low electrical potential difference among said power supply terminals, and other power supply terminals, and protect a semiconductor device from an electrostatic-discharge charge, respectively, Two or more 2nd protection components which intervene between the power supply terminals which supply said low electrical potential difference, and protect from an electrostatic-discharge charge to each power supply terminal, It has two or more supply voltage actuation logical circuit fields constituted by the semiconductor device which operates, respectively with the electrical potential difference of the power supply terminal which supplies a power supply terminal and said low electrical potential difference besides the above. It is the semiconductor device characterized by for said each power supply terminal not having electrical installation mutually at the time of logical circuit actuation, and arranging at least one of said the protection components a center section or near it.

[Claim 2] The 1st power supply terminal and 2nd power supply terminal which supply a power source in said semiconductor device from the outside of a

semiconductor device, The 3rd power supply terminal, 4th power supply terminal, and 5th power supply terminal which supply a power source in said semiconductor device from the outside of said semiconductor device, The 1st supply voltage actuation logical circuit field constituted by the semiconductor device which operates with the electrical potential difference of said 1st power supply terminal and the 2nd power supply terminal, The 2nd supply voltage actuation logical circuit field which operates considering said the 3rd power supply terminal and said 2nd power supply terminal as a power source, The 3rd supply voltage actuation logical circuit field which operates considering said the 4th power supply terminal and said 2nd power supply terminal as a power source, It has the 4th supply voltage actuation logical circuit field which operates considering said the 5th power supply terminal and said 2nd power supply terminal as a power source. Said 2nd power supply terminal is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of said 1st power supply terminal. The potential of said 3rd power supply terminal, said 4th power supply terminal, and said 5th power supply terminal is higher than said 2nd power supply terminal electrical potential difference. Each power supply terminal does not have electrical installation mutually at the time of logical circuit actuation. Between said 1st power supply terminal and the 2nd power supply terminal, Between said 3rd power supply terminal, between the 2nd power supply terminal and the 4th power supply terminal, between the 2nd power supply terminal and the 5th power supply terminal, and the 2nd power supply terminal It connects through the protection component which protects from an electrostatic-discharge charge, respectively. Said 1st power supply terminal, the 3rd power supply terminal, the 4th power supply terminal, and the 5th power supply terminal It is the semiconductor device which is mutually connected through the protection component which protects from an electrostatic-discharge charge to each power supply terminal, and is characterized by arranging at least one of said the protection components a center section or near it.

[Claim 3] Two or more power supply terminals which supply a power source in said semiconductor device from the outside of a semiconductor device, Two or more supply voltage actuation logical circuit fields constituted by the semiconductor device which operates considering the power supply terminal in each set as a power source by said power supply terminal becoming two or more sets of pairs, It has two or more protection components which intervene between the power supply terminals in said each set, and protect from an electrostatic-discharge charge, respectively. It is the semiconductor device characterized by for said each power supply terminal not having electrical installation mutually at the time of logical circuit actuation, and arranging at least one of said the protection components a center section or near it.

[Claim 4] The 1st power supply terminal and 2nd power supply terminal which supply a power source in said semiconductor device from the outside of a semiconductor device, The 3rd power supply terminal which supplies a power source in said semiconductor device from the outside of said semiconductor device, the 4th power supply terminal, the 5th power supply terminal, the 6th power supply terminal, the 7th power supply terminal, and the 8th power supply terminal, The 1st supply voltage actuation logical circuit field constituted by the semiconductor device which operates with the electrical potential difference of said 1st power supply terminal and said 2nd power supply terminal, The 2nd supply voltage actuation logical circuit field which operates considering said the 3rd power supply terminal and said 6th power supply terminal as a power source, The 3rd supply voltage actuation logical circuit field which operates considering said the 4th power supply terminal and said 7th power supply terminal as a power source, It has the 4th supply voltage actuation logical circuit field which operates considering said the 5th power supply terminal and said 8th power supply terminal as a power source. Said 2nd power supply terminal is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of the 1st power supply terminal. Said 3rd power supply terminal, the 4th power supply terminal, the 5th power supply

terminal, the 6th power supply terminal, The 7th power supply terminal and each power supply terminal of the 8th power supply terminal do not have electrical installation mutually at the time of circuit actuation. Said 1st power supply terminal, said 2nd power supply terminal, said the 3rd power supply terminal and said 6th power supply terminal, Said 4th power supply terminal, said 7th power supply terminal, and said the 5th power supply terminal and 8th power supply terminal It connects through the protection component which protects from an electrostatic-discharge charge, respectively. Said 1st supply voltage actuation circuit field, The semiconductor device characterized by at least one of the protection components which interconnect arranging between the power supply terminals of said 2nd supply voltage actuation circuit field, said 3rd supply voltage actuation circuit field, and said 4th supply voltage actuation circuit field a center section or near it.

[Claim 5] Two or more power supply terminals which supply a power source in said semiconductor device from the outside of a semiconductor device, Two or more protection components which intervene between the power supply terminal which supplies a low electrical potential difference among said power supply terminals, and other power supply terminals, and protect a semiconductor device from an electrostatic-discharge charge, respectively, It has two or more supply voltage actuation logical circuit fields constituted by the semiconductor device which operates, respectively with the electrical potential difference of the power supply terminal which supplies a power supply terminal and said low electrical potential difference besides the above. It is the semiconductor device characterized by for said each power supply terminal not having electrical installation mutually at the time of logical circuit actuation, and arranging at least one of said the protection components the center section of the semiconductor device, or near it.

[Claim 6] The 1st power supply terminal and 2nd power supply terminal which supply a power source in a semiconductor device from the outside of a semiconductor device, The 3rd power supply terminal, 4th power supply terminal,

and 5th power supply terminal which supply a power source in a semiconductor device from the outside of a semiconductor device, The 1st supply voltage actuation logical circuit field constituted by the semiconductor device which operates with the electrical potential difference of said 1st power supply terminal and said 2nd power supply terminal, The 2nd supply voltage actuation logical circuit field which operates considering said the 3rd power supply terminal and said 2nd power supply terminal as a power source, The 3rd supply voltage actuation logical circuit field which operates considering said the 4th power supply terminal and said 2nd power supply terminal as a power source, It has the 4th supply voltage actuation logical circuit field which operates considering said the 5th power supply terminal and said 2nd power supply terminal as a power source. Said 2nd power supply terminal is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of the 1st power supply terminal. The potential of said 3rd power supply terminal, said 4th power supply terminal, and said 5th power supply terminal is higher than said 2nd power supply terminal electrical potential difference, each power supply terminal does not have electrical installation mutually at the time of circuit actuation, and said 2nd power supply terminal is received. It is the semiconductor device which interconnects through the protection component which said 1st power supply terminal, said 3rd power supply terminal, said 4th power supply terminal, and said 5th power supply terminal protect from an electrostatic-discharge charge, and is characterized by arranging at least one of said the protection components a center section or near it.

[Claim 7] A protection component is the diode component or MOS which does not pass the current beyond the leakage current at the time of circuit actuation. Claim 1 which consisted of a mold transistor component or a bipolar mold transistor component, claim 2, claim 3, claim 4, semiconductor device according to claim 5 or 6.

[Claim 8] A protection component is said claim 1 respectively formed in the

bottom of current supply wiring to a supply voltage actuation logical circuit field, claim 2, claim 3, claim 4, claim 5, and a semiconductor device according to claim 6 or 7.

[Claim 9] The semi-conductor substrate of the 1st conductivity type, and the 1st high concentration diffusion field which formed on this semi-conductor substrate, is the semi-conductor substrate of said 1st conductivity type, and an opposite conductivity type, and was constituted from a polygonal configuration to said semi-conductor substrate front face, Carry out insertion arrangement of the component isolation region of the fixed distance which counters with the side of the 1st high concentration diffusion field of this polygon, and functions as an electrostatic-discharge charge protection component, and it has said 1st high concentration diffusion field and the 2nd high concentration diffusion field which has a polygonal configuration with this conductivity type. Each side of said 1st high concentration diffusion field prepares the protection component of the polygonal side and an equivalent number by countering with said 2nd high concentration diffusion field and diffusion field of isomorphism. Said protection component formed each side is a semiconductor device characterized by considering as connection used as the energization path of the electrostatic-discharge charge between different power systems.

[Claim 10] The semiconductor device characterized by for two or more circuit fields which have two or more MOS transistor components which have two or more electrical-potential-difference pressure-proofing, and are operating by different supply voltage network existing, and the electrostatic-discharge protection component to at least one supply voltage actuation logical circuit constituting by the MOS transistor component of low-battery pressure-proofing among said two or more MOS transistor components to said two or more circuit fields.

[Claim 11] Claim 1 which the protection component equipped with two or more kinds of electrical-potential-difference proof-pressure MOS transistor components,

claim 2, claim 3, claim 4, claim 5, claim 6, claim 7, claim 8, a semiconductor device according to claim 9 or 10.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which has the protection gestalt which prevents the electrostatic discharge in the semiconductor device which has many power systems with at least three power systems. Moreover, it is related with the semiconductor device which has effectively an electrostatic-discharge prevention gestalt using the high proof-pressure semiconductor device prepared in order to cope with the high voltage signal of the formation of low-battery pressure-proofing of the semiconductor device by detailed-izing of a semiconductor device, and the circumference circuit which connects a semiconductor device.
[0002]
[Description of the Prior Art] Conventionally, as an electrostatic-discharge prevention circuit technique in the semiconductor device which has two or more

power systems, especially a semi-conductor logical circuit, JP,6-5705,B, JP,7-106455,A, JP,8-321586,A, JP,8-316418,A, JP,9-139466,A, and JP,10-50932,A exist. The point of the technique indicated in each official report is following two.
(1) Energize an electrostatic-discharge charge between each power system, and prepare the protection component which secures the path to a grounding point. (An energization path is not asked about the number of stages of the protection component on a par with a serial, parasitism resistance of wiring, etc. (JP,7-106455,A, JP,8-316418,A, JP,9-139466,A).)
(2) by being characterized by forming a common discharge ray to two or more power systems, the electrostatic-discharge charge was energized and the protection element number on the path to a grounding point was set to two -- carry out an electrostatic-discharge protection gestalt (JP,8-321586,A, JP,10-50932,A).
[0003] Each technique is explained below. First, although it is the technique of the conventional example (1), it explains using the circuitry of LSI shown in drawing 11 . In drawing 11 , a VSS power source has four lines, VSS1, VSS2, VSS3, and VSS4, and a VDD power source has four lines, VDD1, VDD2, VDD3, and VDD4. The logical circuit area shown by I1 in the chip area shown by C1 outside shows the area of the LSI circumference. Here, supposing it grounds VDD1 temporarily and a forward electrostatic-discharge charge is impressed to VDD3, positive charge goes to the touch-down edge. At this time, one of the energization paths passes the protection component of G23 from VDD3, and it passes along wiring of VDD2, passes the protection component of G22 further, and flows to the earth terminal of VDD1. As another energization path, the protection component of G11 is passed from VDD3, and it passes along wiring of VSS1, and reaches to the earth terminal of VDD1 through the protection component of G1 further. It determines which path is energized by the resistance component of the property of a protection component, and a wiring path, and the capacity component. Although this example showed the case where energized two protection components and an electrostatic-discharge charge was missed,

by LSI which has two or more electrical power systems similarly, more protection components will be energized and an electrostatic-discharge charge will be missed.

[0004] Next, although it is the circuit technique of the conventional example (2), the example of LSI circuitry is shown to drawing 12 . The discharge ray LA 1 which is newly common wiring for discharge to the method of drawing 11 is formed out of the external terminal around chip area, and the protection component G40 is formed between an external terminal and a discharge ray LA 1. By this method, it considers that an electrostatic-discharge charge misses a charge through the common discharge ray LA 1, and however an electrical power system may exist and it may impress an electrostatic-discharge charge to which terminal, it becomes possible to miss a charge only through a maximum of two protection components.

[0005] the N+ diffusion field n1 fundamentally shown in drawing 5 by the CMOS process on the other hand although it came out about the component configuration of an electrostatic-discharge protection component, and a P-mold -- it becomes the Nch mold MOS transistor configuration which consists of N+ diffusion fields n1, N+ diffusion fields n2, and the gates Ga1 shown by the NPN bipolar configuration which consists of a well p2, an N+ diffusion field n2, and a P+ diffusion field p1, or drawing 6 . Of course, the PNP bipolar configuration and Pch mold MOS transistor configuration which made the polarity of a diffusion field and a well reverse are also used by the case. When these circuits are used as a device layout pattern, there is a Kushigata configuration of drawing 7 generally known and drawing 8 (A). Moreover, the mesh gate protection component which made the gate electrode (or separation area of a diffusion field) of a transistor the shape of a mesh, and the protection component configuration further considered as the polygon or the circular gate configuration are proposed.

[0006] In order to, improve the property at the time of missing the electrostatic-discharge charge of a protection component on the other hand and to make protection component area small, addition of a production process and addition

of a mask pattern are performed.

[0007]

[Problem(s) to be Solved by the Invention] In LSI which has two or more electrical power systems on 1 device, the technical problem which this invention solves minimizes the increment in area for the device protection from an electrostatic-discharge charge, and performs it.

[0008] First, a protection component is explained first and the detail of a technical problem is shown after that. The configuration of a protection component is the bipolar mold transistor or MOS it was indicated by drawing 5 and drawing 6 that already stated. It consists of mold transistors. When LSI is performing the usual actuation, with the bipolar mold transistor of drawing 5 , a collector terminal is connected with the substrate used as a base terminal, and since the reverse bias pressure-proofing of the semi-conductor junction of N+ and P- constituted by an emitter terminal and the base terminal is an electrical potential difference more than absolute maximum rating, the current beyond the leakage current is not generated. On the other hand, it is MOS. In the case of a mold transistor, the gate electrode is always turned off, when LSI is performing the usual actuation, since it connects with the source of a transistor. MOS The actuation at the time of electrostatic-discharge charge impression of the protection component at the time of constituting from a mold transistor becomes being the same as that of a bipolar transistor. An electrostatic-discharge charge has straight polarity or negative polarity, and, therefore, potential and the amount of charges differ from the transient characteristic on a time-axis for an electrification object or a discharge path. When explaining actuation of a protection component, the electrostatic discharge of positive charge and a negative charge is shown.

[0009] MOS of drawing 6 A property when the electrostatic-discharge charge which has straight polarity in the drain D1 of a mold transistor is impressed is shown in the property graph of drawing 10 . It becomes a reverse bias, and the potential difference of a drain D1 and the source S1 (substrate potential) reaches fixed potential, and sometimes produces avalanche breakdown, and the diode

which consists of the diffusion fields D1 and the P-substrates p2 of N+ begins to pass a current from a drain to a substrate and the source. At this time, the potential difference of a drain D1 and the source S1 is mostly fixed by the low battery from the potential which produced avalanche breakdown. Furthermore, if drain D1 potential is raised, destruction of the protection component itself will arise at the time of the secondary breakdown current shown in the property graph of drawing 10 , and secondary breakdown voltage. The property of the protection component shown by drawing 10 is also called snapback property, and serves as avalanche breakdown potential about 10V-15V in a detailed process in recent years, and secondary breakdown voltage and a current are dozens ofmA/micrometer per unit gate width before and after 2 - 3V. It becomes extent. On the other hand, when the electrostatic-discharge charge which has negative polarity in the drain D1 of a MOS transistor is impressed, the diode of N+ diffusion field D1 and the P-substrate p2 serves as a forward bias, and the potential difference between the both-ends children of diode is about 0.7V. Potential is fixed almost uniformly in a current with extent at the beginning of a sink. There are many amounts of currents which can generally pass the forward bias.

[0010] It is important to take into consideration the parasitic element component of wiring from an external terminal to a protection component and the parasitic element component of wiring to other usual circuits in addition to the above protection component property. Although the amount of currents by the electrostatic-discharge charge generally number A Flows, it is required to consider as the value to which the potential of an energization path is determined by the sum of the fixed potential at the time of the rise and protection component of potential by the parasitism resistance component energizing, and this potential does not exceed pressure-proofing of a semiconductor device. Moreover, to timing until a protection component begins to pass a current, in order [which does not require potential for other semiconductor devices] to delay a potential rise like, also making a capacity component add by the case is considered. By

this invention, it solves mainly about the three following points to the gestalt which protects a semiconductor device from the above electrostatic-discharge charge.

[0011] An electrostatic-discharge charge is energized between each power system of the conventional example (1) explained in the Prior art, and the technical problem of a protection gestalt that the path to a grounding point is secured is explained using drawing 11 . First, temporarily, supposing it impresses an electrostatic-discharge charge to OUT1 by making VDD3 into a grounding point, a charge will reach even to VDD3 terminal through the protection component G2, the protection component G21, and the protection component G24. If the fixed electrical potential difference at the time of a protection component energizing is set to 2V, since it has a three-element serial, the potential difference of 6V has been produced. Parasitism resistance of the path to energize is 100 micrometers in sheet resistance 0.1ohm/**, and a wire length about 20mm (the semiconductor device of 10mm**, the terminal and assumption which counter), and wiring width of face. It will be set to about 20ohms if it carries out.

[0012] If the current by the electrostatic-discharge charge is set to 1A, the potential of 20V will occur in wiring parasitism resistance. The potential by the protection component and wiring parasitism resistance is total 26V. It becomes. Here, since diode L1P1D1 formed of the substrate and diffusion field of Pch transistor L1P1 of an internal circuitry (logical circuit field L1) will pass a current only by the potential difference of 0.7V with forward direction potential supposing the electrostatic-discharge charge has negative polarity, it can assume that the potential beyond 16V is built over the gate voltage of Pch transistor L3P1 of the logical circuit field L3. MOS in a detailed process in recent years If instant gate pressure-proofing of a transistor considers as about 16V, it will be considered easily that gate destruction of a Pch transistor arises.

[0013] If two or more power systems are furthermore assumed, two or more protection components will be connected with a serial, and we are anxious about

the potential difference occurring more.

[0014] On the other hand, a detail is explained about the conventional example (2) explained in the Prior art using drawing 12 . In the case of drawing 12 , the number of stages of the protection component of the path which misses an electrostatic-discharge charge is reduced. Therefore, having formed the common discharge ray LA 1 separately can call it the greatest description. However a power system may increase, since a maximum of two protection components are [only connecting with a serial, and], the rise of the electrical potential difference by the protection component is only 4V in an above-mentioned example. However, the increment in layout area cannot be denied by being unable to reduce parasitism resistance of the discharge ray on the path which misses an electrostatic-discharge charge also by this method, and preparing wiring separately.

[0015] As a protection component layout, there are the Kushigata layout configuration and mesh mold layout with either configuration of the bipolar mold transistor of drawing 5 and the MOS transistor of drawing 6 of drawing 7 and drawing 8 (A). N+ semi-conductor diffusion field, and p1-p3 n1-n8 P+ semi-conductor diffusion field, A bipolar mold transistor emitter terminal and C1 E1 A bipolar mold transistor collector terminal, D1 is MOS. A mold transistor drain terminal and S1 MOS transistor source terminal, Ga1 and Ga2 As for semiconductor device keepout areas other than a protection component near the protection component, and v1 and v2, for a MOS transistor gate terminal and r1, substrate resistance and r2 are [a diffusion field-aluminum wiring contact component and vp1] gate electrode-aluminum wiring contact components.

[0016] Although the Kushigata layout configuration is a layout currently used conventionally and a mesh mold is the comparatively new layout technique, all are the protection components between two potential systems. Here, the protection component layout area between 5 electrical power systems is calculated using drawing 8 (A). It is 200 micrometers about the width of face of the side of the diffusion field which counters. It is 0.5 micrometers about spacing

of the diffusion field which counters. When forming a protection component in the mutual one between [of five lines] power sources, with the Kushigata protection component, it becomes the configuration of drawing 8 (A). For other diffusion fields of the diffusion field of a protection component, if width of face of the side which does not counter is set to 10 micrometers, the protection component layout area of drawing 8 (A) is 200 micrometers to 115 micrometers and a lengthwise direction in a longitudinal direction. Becoming, a gross area is 23000 micrometers. 2 It becomes.

[0017] This invention solves the technical problem of description, and proposes the semiconductor device of the gestalt which can be carried out easily.

[0018] Therefore, any electrostatic-discharge charges are offering the semiconductor device which becomes possible [reducing the parasitism resistance components of the energization path of an electrostatic-discharge charge by considering a protection component as three or less steps of connection at a serial, and arranging the protection component between power sources on an LSI core or the outskirts of it] in LSI to which the 1st purpose of this invention has many power systems.

[0019] It is offering the semiconductor device which the 2nd purpose's can secure the energization path of the electrostatic-discharge charge which minded the protection component by making into a terminal node power-source wiring common when at least one common power source's exists by LSI which has many power systems, can carry out the number of stages from which a protection component's becomes in-series at this time to four steps, and can reduce a protection component total.

[0020] It is offering the semiconductor device which enables reduction of the protection component area by the 3rd purpose's making the configuration of a protection component a polygon, and making connection of the protection component of each side another electrical power system.

[0021] The 4th purpose is offering the semiconductor device which can miss smoothly the static electricity charge by low-battery pressure-proofing and the

low-battery clamp component to an earth terminal using having two electrical-potential-difference pressure-proofing on a semiconductor device having been generalized effectively, when the signal level of the semiconductor device circumference does not change to the fall of the supply voltage of the semiconductor device by detailed-izing in recent years of operation.

[0022]

[Means for Solving the Problem] Two or more power supply terminals with which a semiconductor device according to claim 1 supplies a power source in a semiconductor device from the outside of a semiconductor device, Two or more 1st protection components which intervene between the power supply terminal which supplies a low electrical potential difference among power supply terminals, and other power supply terminals, and protect a semiconductor device from an electrostatic-discharge charge, respectively, Two or more 2nd protection components which intervene between the power supply terminals which supply a low electrical potential difference, and protect from an electrostatic-discharge charge to each power supply terminal, It has two or more supply voltage actuation logical circuit fields constituted by the semiconductor device which operates, respectively with the electrical potential difference of the power supply terminal which supplies other power supply terminals and low electrical potential differences. It is characterized by for each power supply terminal not having electrical installation mutually at the time of logical circuit actuation, and arranging at least one of the protection components a center section or near it.

[0023] According to the semiconductor device according to claim 1, the path which misses impression of the charge by static electricity to an earth terminal is securable by restricting the number of stages of a protection component, and arranging a protection component, using power-source wiring into an actual circuit effectively.

[0024] The 1st power supply terminal and 2nd power supply terminal with which a semiconductor device according to claim 2 supplies a power source in a semiconductor device from the outside of a semiconductor device, The 3rd

power supply terminal, 4th power supply terminal, and 5th power supply terminal which supply a power source in a semiconductor device from the outside of a semiconductor device, The 1st supply voltage actuation logical circuit field constituted by the semiconductor device which operates with the electrical potential difference of the 1st power supply terminal and the 2nd power supply terminal, The 2nd supply voltage actuation logical circuit field which operates considering the 3rd power supply terminal and 2nd power supply terminal as a power source, The 3rd supply voltage actuation logical circuit field which operates considering the 4th power supply terminal and 2nd power supply terminal as a power source, It has the 4th supply voltage actuation logical circuit field which operates considering the 5th power supply terminal and 2nd power supply terminal as a power source. The 2nd power supply terminal is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of the 1st power supply terminal. The potential of the 3rd power supply terminal, the 4th power supply terminal, and the 5th power supply terminal is higher than the 2nd power supply terminal electrical potential difference. Each power supply terminal does not have electrical installation mutually at the time of logical circuit actuation. Between the 1st power supply terminal and the 2nd power supply terminal, Between the 3rd power supply terminal, between the 2nd power supply terminal and the 4th power supply terminal, between the 2nd power supply terminal and the 5th power supply terminal, and the 2nd power supply terminal It connects through the protection component which protects from an electrostatic-discharge charge, respectively. The 1st power supply terminal, the 3rd power supply terminal, the 4th power supply terminal, and the 5th power supply terminal It connects mutually through the protection component which protects from an electrostatic-discharge charge to each power supply terminal, and is characterized by arranging at least one of the protection components a center section or near it.
[0025] According to the semiconductor device according to claim 2, there is the same effectiveness as claim 1.

[0026] Two or more power supply terminals with which a semiconductor device according to claim 3 supplies a power source in a semiconductor device from the outside of a semiconductor device, Two or more supply voltage actuation logical circuit fields constituted by the semiconductor device which operates considering the power supply terminal in each set as a power source by a power supply terminal becoming two or more sets of pairs, It has two or more protection components which intervene between the power supply terminals in each set, and protect from an electrostatic-discharge charge, respectively. It is characterized by for each power supply terminal not having electrical installation mutually at the time of logical circuit actuation, and arranging at least one of the protection components a center section or near it.
[0027] According to the semiconductor device according to claim 3, there is the same effectiveness as claim 1.
[0028] The 1st power supply terminal and 2nd power supply terminal with which a semiconductor device according to claim 4 supplies a power source in a semiconductor device from the outside of a semiconductor device, The 3rd power supply terminal which supplies a power source in a semiconductor device from the outside of a semiconductor device, the 4th power supply terminal, the 5th power supply terminal, the 6th power supply terminal, the 7th power supply terminal, and the 8th power supply terminal, The 1st supply voltage actuation logical circuit field constituted by the semiconductor device which operates with the electrical potential difference of the 1st power supply terminal and the 2nd power supply terminal, The 2nd supply voltage actuation logical circuit field which operates considering the 3rd power supply terminal and 6th power supply terminal as a power source, The 3rd supply voltage actuation logical circuit field which operates considering the 4th power supply terminal and 7th power supply terminal as a power source, It has the 4th supply voltage actuation logical circuit field which operates considering the 5th power supply terminal and 8th power supply terminal as a power source. The 2nd power supply terminal is a power supply terminal which supplies a low electrical potential difference compared with

the electrical potential difference of the 1st power supply terminal. The 3rd power supply terminal, the 4th power supply terminal, the 5th power supply terminal, the 6th power supply terminal, The 7th power supply terminal and each power supply terminal of the 8th power supply terminal do not have electrical installation mutually at the time of circuit actuation. A power supply terminal, the 2nd power supply terminal and the 3rd power supply terminal, the 6th power supply terminal and the 4th power supply terminal, the 7th power supply terminal, and the 1st power supply terminal and 8th power supply terminal [5th] It connects through the protection component which protects from an electrostatic-discharge charge, respectively. The 1st supply voltage actuation circuit field, It is characterized by at least one of the protection components which interconnect arranging between the power supply terminals of the 2nd supply voltage actuation circuit field, the 3rd supply voltage actuation circuit field, and the 4th supply voltage actuation circuit field a center section or near it.

[0029] According to the semiconductor device according to claim 4, there is the same effectiveness as claim 1.

[0030] Two or more power supply terminals with which a semiconductor device according to claim 5 supplies a power source in a semiconductor device from the outside of a semiconductor device, Two or more protection components which intervene between the power supply terminal which supplies a low electrical potential difference among power supply terminals, and other power supply terminals, and protect a semiconductor device from an electrostatic-discharge charge, respectively, It has two or more supply voltage actuation logical circuit fields constituted by the semiconductor device which operates, respectively with the electrical potential difference of the power supply terminal which supplies other power supply terminals and low electrical potential differences. It is characterized by for each power supply terminal not having electrical installation mutually at the time of logical circuit actuation, and arranging at least one of the protection components a center section or near it.

[0031] When it is the logical circuit configuration which shared one of one

electrical power system among many electrical power systems in a semiconductor device according to the semiconductor device according to claim 5, it is possible to reduce a protection element number in addition to the effectiveness of claim 1.

[0032] The 1st power supply terminal and 2nd power supply terminal with which a semiconductor device according to claim 6 supplies a power source in a semiconductor device from the outside of a semiconductor device, The 3rd power supply terminal, 4th power supply terminal, and 5th power supply terminal which supply a power source in a semiconductor device from the outside of a semiconductor device, The 1st supply voltage actuation logical circuit field constituted by the semiconductor device which operates with the electrical potential difference of the 1st power supply terminal and the 2nd power supply terminal, The 2nd supply voltage actuation logical circuit field which operates considering the 3rd power supply terminal and 2nd power supply terminal as a power source, The 3rd supply voltage actuation logical circuit field which operates considering the 4th power supply terminal and 2nd power supply terminal as a power source, It has the 4th supply voltage actuation logical circuit field which operates considering the 5th power supply terminal and 2nd power supply terminal as a power source. The 2nd power supply terminal is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of the 1st power supply terminal. The potential of the 3rd power supply terminal, the 4th power supply terminal, and the 5th power supply terminal is higher than the 2nd power supply terminal electrical potential difference, each power supply terminal does not have electrical installation mutually at the time of circuit actuation, and the 2nd power supply terminal is received. It interconnects through the protection component which the 1st power supply terminal, the 3rd power supply terminal, the 4th power supply terminal, and the 5th power supply terminal protect from an electrostatic-discharge charge, and is characterized by arranging at least one of the protection components the center section of the semiconductor device, or near it.

[0033] According to the semiconductor device according to claim 6, there is the same effectiveness as claim 5.
[0034] A semiconductor device according to claim 7 is the diode component or MOS to which a protection component does not pass the current beyond the leakage current in claim 1, claim 2, claim 3, claim 4, claim 5, or claim 6 at the time of circuit actuation. It consists of a mold transistor component or a bipolar mold transistor component.
[0035] According to the semiconductor device according to claim 7, there is the same effectiveness as claim 1, claim 2, claim 3, claim 4, claim 5, or claim 6.
[0036] In claim 1, claim 2, claim 3, claim 4, claim 5, claim 6, or claim 7, as for a semiconductor device according to claim 8, a protection component is respectively formed in the bottom of current supply wiring to a supply voltage actuation logical circuit field.
[0037] According to the semiconductor device according to claim 8, there is the same effectiveness as claim 1, claim 2, claim 3, claim 4, claim 5, claim 6, or claim 7.
[0038] The 1st high concentration diffusion field which formed the semiconductor device according to claim 9 on the semi-conductor substrate of the 1st conductivity type, and this semi-conductor substrate, is the semi-conductor substrate of the 1st conductivity type, and an opposite conductivity type, and was constituted from a polygonal configuration to the semi-conductor substrate front face, Carry out insertion arrangement of the component isolation region of the fixed distance which counters with the side of the 1st high concentration diffusion field of this polygon, and functions as an electrostatic-discharge charge protection component, and it has the 1st high concentration diffusion field and the 2nd high concentration diffusion field which has a polygonal configuration with this conductivity type. It is characterized by considering the protection component which prepares the protection component of the polygonal side and an equivalent number, and is formed each side as connection used as the energization path of the electrostatic-discharge charge between different power systems, when each

side of the 1st high concentration diffusion field counters with the 2nd high concentration diffusion field and the diffusion field of isomorphism.

[0039] According to the semiconductor device according to claim 9, it becomes possible to reduce area further by considering the component configuration of a multi-electrical power system protection component as a polygonal mesh configuration.

[0040] It is characterized by for two or more circuit fields which have two or more MOS transistor components which have two or more electrical-potential-difference pressure-proofing, and are operating by different supply voltage network existing, and the electrostatic-discharge protection component to at least one supply voltage actuation logical circuit constituting a semiconductor device according to claim 10 by the MOS transistor component of low-battery pressure-proofing among two or more MOS transistor components to two or more circuit fields.

[0041] According to the semiconductor device according to claim 10, when the signal level of the semiconductor device circumference does not change to the fall of the supply voltage of the semiconductor device by detailed-izing in recent years of operation, it is possible to reduce the potential difference at the time of having two electrical-potential-difference pressure-proofing on a semiconductor device energizing for a protection component, using to have become common effectively, and the potential difference rise from the static electricity charge impression terminal to an earth terminal can be lowered.

[0042] As for a semiconductor device according to claim 11, a protection component is equipped with two or more kinds of electrical-potential-difference proof-pressure MOS transistor components in claim 1, claim 2, claim 3, claim 4, claim 5, claim 6, claim 7, claim 8, claim 9, or claim 10.

[0043] According to the semiconductor device according to claim 11, there is the same effectiveness as claim 1, claim 2, claim 3, claim 4, claim 5, claim 6, claim 7, claim 8, claim 9, or claim 10.

[0044]

[Embodiment of the Invention] The operation gestalt of the technique using the aforementioned means which carries out technical-problem solution is shown below to the technical problem of the conventional technique.

[0045] (Gestalt 1 of operation) The gestalt of the 1st operation corresponding to claims 1-4 of this invention is explained using drawing 1 and drawing 2 . Drawing 1 and drawing 2 show the chip of LSI typically, respectively. In these drawings VDD1-VDD4, and VSS1-VSS4 A power system, A signal input terminal, and OUT1-OUT4 IN1-IN4 A signal output terminal, IO-P1 - IO-P8, IO-N1 - IO-N8 of the logical circuit field where an electrostatic-discharge protection component is supplied to an input signal, the component from which an output signal circuit is constituted, and G1-G36 from each electrical power system, and a power source is supplied to L1-L4, and C11 are [a semiconductor device frame and I1] internal logical circuit fields.

[0046] It had the logical circuit part shown by I1 in the LSI chip shown by C1, and the input / output terminal, or the current supply terminal of an external signal is prepared around the chip (in this invention, the convention has not been carried out to profit about preparing a terminal in the LSI exterior). Although semiconductor devices, such as a transistor, are connected to each terminal needless to say, the protection component which protects a semiconductor device from excessive charges, such as external static electricity, with it is prepared. A semiconductor device is IO-P1 and IO-P2.... They are IO-P8, IO-N1, and IO-N2.... It is shown by IO-N8. The protection component connected is G1, G2, and G3.... G36 shows. The term of a Prior art already shows the function of a protection component. Some which serve as the description in this invention are to form the protection components G25 and G26 in drawing 1 in the logical circuit part inside [I1] the chip of LSI. With the gestalt of drawing 11 mentioned already by the Prior art, as already stated, when it had two or more electrical power systems, and it prepared two or more protection components in a serial and big parasitism resistance attachment ****** made an electrostatic-discharge charge energize, it already stated that it is possible to give an excessive charge in part to

a semiconductor device. The case where an electrostatic-discharge charge was impressed to OUT1 by making VDD3 into a grounding point, using drawing 11 as an example was explained. The same conditions show the case where the configuration of drawing 1 is used. When VDD3 is grounded and the seal of approval of the electrostatic-discharge charge is carried out to OUT1, a charge energizes the protection components G4 and G25, and reaches VDD3. the potential produced by the protection component connected to the serial at this time -- a total of 4 -- V it is . Moreover, since the protection component is prepared in the logical circuit part inside [I1] a chip, a wire length becomes short. If it is a chip size equivalent to said example, it will be considered wire-length extent of 10mm. Moreover, it is 100 micrometers about the wiring width of face of the power-source trunk of LSI inside LSI. Parasitism resistance is 10ohms, when it carries out, it laps with power-source wiring and a protection component is formed. Supposing the current of 1A arises for the path which makes an electrostatic-discharge charge energize, the potential difference over the earth terminal of a charge impression terminal is 14V. Although the protection component of the adjoining electrical power system is good to arrange to the field which adjoins like the protection components G21, G22, G23, and G24, the thing which were mentioned above to the electrical power system field not adjoining and for which the impedance of a component is lowered like is important.

[0047] The circuit shown in drawing 2 is the case where the common power source VSS1 of drawing 1 is divided to four VSS(s). Also in this case, similarly, the number of the protection component by which one is connected to a serial by having formed the protection components G25, G26, G31-G36 in the logical circuit part inside [I1] a chip to a different electrical power system not adjoining is reduced, and wiring parasitism resistance is reduced by one side.

[0048] Thus, the 1st power supply terminal (VDD1) and 2nd power supply terminal (VSS1) which supply a power source in a semiconductor device from the outside of a semiconductor device in drawing 1 with the gestalt of the 1st operation, The 3rd power supply terminal (VDD2), 4th power supply terminal

(VDD3), and 5th power supply terminal (VDD4) which supply a power source in a semiconductor device from the outside of a semiconductor device, The 1st supply voltage actuation logical circuit field (L1) constituted by the semiconductor device which operates with the electrical potential difference of the 1st power supply terminal (VDD1) and the 2nd power supply terminal (VSS1), The 2nd supply voltage actuation logical circuit field (L2) which operates considering the 3rd power supply terminal (VDD2) and 2nd power supply terminal (VSS1) as a power source, The 3rd supply voltage actuation logical circuit field (L3) which operates considering the 4th power supply terminal (VDD3) and 2nd power supply terminal (VSS1) as a power source, It has the 4th supply voltage actuation logical circuit field (L4) which operates considering the 5th power supply terminal (VDD4) and 2nd power supply terminal (VSS1) as a power source. The 2nd power supply terminal (VSS1) is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of the 1st power supply terminal (VDD1). The potential of the 3rd power supply terminal (VDD2), the 4th power supply terminal (VDD3), and the 5th power supply terminal (VDD4) is higher than the 2nd power supply terminal (VSS1) electrical potential difference. Each power supply terminal does not have electrical installation mutually at the time of logical circuit actuation. Between the 1st power supply terminal (VDD1) and the 2nd power supply terminal (VSS1), Between the 3rd power supply terminal (VDD2), between the 2nd power supply terminal (VSS1) and the 4th power supply terminal (VDD3), and the 2nd power supply terminal (VSS1), Between the 5th power supply terminal (VDD4) and the 2nd power supply terminal (VSS1) It connects through the protection component which protects from an electrostatic-discharge charge, respectively. The 1st power supply terminal (VDD1), It connected mutually through the protection component which protects from an electrostatic-discharge charge to each power supply terminal, and the 3rd power supply terminal (VDD2), the 4th power supply terminal (VDD3), and the 5th power supply terminal (VDD4) arrange at least one of the protection components a center section or near it.

[0049] Moreover, the 1st power supply terminal (VDD1) and 2nd power supply terminal (VSS1) which supply a power source in a semiconductor device from the outside of a semiconductor device in drawing 2 , The 3rd power supply terminal which supplies a power source in a semiconductor device from the outside of a semiconductor device (VDD2), The 4th power supply terminal (VDD3), the 5th power supply terminal (VDD4), the 6th power supply terminal (VSS2), the 7th power supply terminal (VSS3), and the 8th power supply terminal (VSS4), The 1st supply voltage actuation logical circuit field (L1) constituted by the semiconductor device which operates with the electrical potential difference of the 1st power supply terminal (VDD1) and the 2nd power supply terminal (VSS1), The 2nd supply voltage actuation logical circuit field (L2) which operates considering the 3rd power supply terminal (VDD2) and 6th power supply terminal (VSS2) as a power source, The 3rd supply voltage actuation logical circuit field (L3) which operates considering the 4th power supply terminal (VDD3) and 7th power supply terminal (VSS3) as a power source, It has the 4th supply voltage actuation logical circuit field (L4) which operates considering the 5th power supply terminal (VDD4) and 8th power supply terminal (VSS4) as a power source. The 2nd power supply terminal (VSS1) is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of the 1st power supply terminal (VDD1). The 3rd power supply terminal (VDD2), the 4th power supply terminal (VDD3), the 5th power supply terminal (VDD4), The 6th power supply terminal (VSS2), the 7th power supply terminal (VSS3), and each power supply terminal of the 8th power supply terminal (VSS4) do not have electrical installation mutually at the time of circuit actuation. A power supply terminal (VDD1), the 2nd power supply terminal (VSS1), the 1st power supply terminal (VDD2) and 6th power supply terminal (VSS2), [3rd] A power supply terminal (VDD3), the 7th power supply terminal (VSS3), and the 4th power supply terminal (VDD4) and 8th power supply terminal (VSS4) [5th] It connects through the protection component which protects from an electrostatic-discharge charge, respectively. The 1st supply

voltage actuation circuit field (L1), At least one of the protection components which interconnect arranges between the power supply terminals of the 2nd supply voltage actuation circuit field (L2), the 3rd supply voltage actuation circuit field (L3), and the 4th supply voltage actuation circuit field (L4) a center section or near it.

[0050] (Gestalt 2 of operation) The gestalt of the 2nd operation corresponding to claims 5 and 6 of this invention when an electrical power system increases further in the gestalt of the 1st operation is shown in drawing 4 . G37 and G38 are protection components, and others are the same as the gestalt of the 1st operation.

[0051] First, drawing 3 shows the insertion gestalt of the protection component to the electrical power system not adjoining. 20 protection components G37 inserted in the logical circuit part inside [I1] a chip exist. It is effective to prepare a protection component in the interior I1 of a chip to the electrical power system which does not adjoin as the gestalt of the 1st operation already described, when reducing the number of stages of the protection component linked to reducing parasitism resistance components and a serial, and when protecting a semiconductor device from an electrostatic-discharge charge, it is effective. However, increase of the chip area of LSI arises because a protection component increases by the increment in a power system.

[0052] Then, when there is at least one common power source, the case where the number of protection components is reduced by making the share power source into a terminal node is shown in drawing 4 . In drawing 4 , since VSS1 is used as the share power source, the number of the protection component G38 is reduced by only eight lines. The power supply terminal which exists like the case of the above-mentioned example is grounded, and suppose that the electrostatic-discharge charge was impressed to the terminal of arbitration. In the above-mentioned example, when an electrostatic-discharge charge was impressed to an output terminal OUT1, the charge was energized to VDD1 power-source wiring through the protection component, and the charge was missed through the

protection component to the grounding point of the earth terminal of VDD3. Energizing the protection component G38 by the side of VDD5 further once through VSS1 wiring, after a charge's energizing to power-source wiring of VDD1 and energizing for one protection component G38 by the case where VDD5 of drawing 4 is used as an earth terminal as an example of the gestalt of the 2nd operation, a charge will escape at the touch-down edge VDD5. Although drawing 1 showed share power-source wiring and it usually wires near the periphery of a chip C1 like about invention shown with the gestalt of the 2nd operation It is effective when forming an electrostatic-discharge path, in case the parasitism resistance components at the time of forming the protection between power sources in the electrical power system which counters on a chip can be reduced, it prepares in the interior of the chip in which the external terminal of a common power source was shown by I1 and a DC power supply is supplied.

[0053] Thus, the semiconductor device in the gestalt of the 2nd operation It has the 1st power supply terminal (VDD1) and 2nd power supply terminal (VSS1) which supply a power source in a semiconductor device from the outside of a semiconductor device. The 1st supply voltage actuation logical circuit field constituted by the semiconductor device which the 2nd power supply terminal (VSS1) is a power supply terminal which supplies a low electrical potential difference compared with the electrical potential difference of the 1st power supply terminal (VDD1), and operates with the electrical potential difference of the two above-mentioned power supply terminals, In addition, it has the 3rd power supply terminal (VDD2), 4th power supply terminal (VDD3), 5th power supply terminal (VDD4), 6th power supply terminal (VDD5), 7th power supply terminal (VDD6), and 8th power supply terminal (VDD7) which supply a power source in a semiconductor device from the outside of a semiconductor device. The potential of the 3rd power supply terminal (VDD2), the 4th power supply terminal (VDD3), the 5th power supply terminal (VDD4), the 6th power supply terminal (VDD5), the 7th power supply terminal (VDD6), and the 8th power supply terminal (VDD7) is higher than the 2nd power supply terminal (VSS1)

electrical potential difference. The 2nd supply voltage actuation logical circuit field which each power supply terminal does not have electrical installation at the time of circuit actuation, and operates considering the 3rd power supply terminal (VDD2) and 2nd power supply terminal (VSS1) as a power source, The 3rd supply voltage actuation logical circuit field which operates considering the 4th power supply terminal (VDD3) and 2nd power supply terminal (VSS1) as a power source, The 4th supply voltage actuation logical circuit field which operates considering the 5th power supply terminal (VDD4) and 2nd power supply terminal (VSS1) as a power source, The 5th supply voltage actuation logical circuit field which operates considering the 6th power supply terminal (VDD5) and 2nd power supply terminal (VSS1) as a power source, The 6th supply voltage actuation logical circuit field which operates considering the 7th power supply terminal (VDD6) and 2nd power supply terminal (VSS1) as a power source, Have the 7th supply voltage actuation logical circuit field which operates considering the 8th power supply terminal (VDD7) and 2nd power supply terminal (VSS1) as a power source, and the 2nd power supply terminal (VSS1) is received. The 1st power supply terminal (VDD1), the 3rd power supply terminal (VDD2), the 4th power supply terminal (VDD3), The 5th power supply terminal (VDD4), the 6th power supply terminal (VDD5), the 7th power supply terminal (VDD6), The 8th power supply terminal (VDD7) interconnected through the protection component which protects a semiconductor device from an electrostatic-discharge charge, and arranges at least one of the protection components a center section or near it.

[0054] When at least one common power source exists by LSI which has many power systems according to the gestalt of the 2nd operation, the protection component number of stages by which secures the energization path of the electrostatic-discharge charge which minded the protection component by making common power-source wiring into a terminal node, and series connection is carried out between different power sources can be carried out to to a maximum of two steps, and a protection component total can be reduced. However, a number of stages can be carried out to three steps, four steps, or

more than it.

[0055] In addition, a protection component is the diode component or MOS which does not pass the current beyond the leakage current at the time of circuit actuation of a semiconductor device. It consists of a mold transistor component or a bipolar mold transistor component. Moreover, a protection component is respectively formed in the bottom of current supply wiring to a supply voltage actuation logical circuit field.

[0056] (Gestalt 3 of operation) Drawing 8 and drawing 9 explain the gestalt of the 3rd operation corresponding to claim 9 of this invention. Invention of claim 9 constitutes each side of the protection component which consists of polygonal diffusion fields as a power-sources protection component of one, and serves as a configuration shown in drawing 8 (B) and drawing 9 as an example. It is drawing 9 which expanded especially the field of the protection component which drawing 8 (B) forms the power-sources protection component of five lines, and is shown by G39. A, B, C, D, E, and F which are contained in eye each measure by drawing 8 (B) show a power system, and the inside of eye measure is a diffusion field. Each side of a diffusion field serves as a protection component between the power sources which counter. The gestalt of operation of this invention is explained like area count of the protection component layout of Kushigata shown by Object of the Invention. In the protection component layout of Kushigata, the diffusion field had countered by width of face of 200 micrometers. Area count is performed on the conditions made into the opposite width of face of the same diffusion field also with a multi-power-source mesh mold protection component. the thing which were shown in drawing 8 (B) when one side of eye measure it is in a mesh was set to 5 micrometers and which eye measure considers as 12 length and 22 width like -- diffusion field opposite width of face of 200 micrometers The above is secured. If spacing of the diffusion field which counters is set to 0.5 micrometers, area will serve as 7892.75 micrometer2. The layout area of the protection component layout of above-mentioned Kushigata is 23000 micrometers. If it compares, it will become about 34.3% of layout area,

and will become small area very much.

[0057] Thus, the 1st high concentration diffusion field which formed on the semi-conductor substrate of the 1st conductivity type, and this semi-conductor substrate, is the semi-conductor substrate of the 1st conductivity type, and an opposite conductivity type, and was constituted from a gestalt of the 3rd operation in the polygonal configuration to the semi-conductor substrate front face (A), Carry out insertion arrangement of the component isolation region of the fixed distance which counters with the side of the 1st high concentration diffusion field (A) of this polygon, and functions as an electrostatic-discharge charge protection component, and it has the 1st high concentration diffusion field (A) and the 2nd high concentration diffusion field (B, C, D, E) which has a polygonal configuration with this conductivity type. When each side of the 1st high concentration diffusion field (A) counters with the 2nd high concentration diffusion field (B, C, D, E) and the diffusion field of isomorphism, the protection component of the polygonal side and an equivalent number is prepared, and the protection component formed each side is considered as connection used as the energization path of the electrostatic-discharge charge between different power systems.

[0058] It enables this to reduce area further by considering the component configuration of a multi-electrical power system protection component as a polygonal mesh configuration. The number of angles of the above-mentioned polygon is included, also when it becomes infinite and a high concentration diffusion field becomes circular.

[0059] (Gestalt 4 of operation) The gestalt of the 4th operation corresponding to claim 10 of this invention is explained using drawing 10 . Setting to drawing 10 , LB1 and LB2 are the gate effective length and Ga2. A MOS transistor gate terminal and others are the same with having explained other drawings.

[0060] That whose standard actuation supply voltage of a CMOS semiconductor device even 0.6-micrometer process generation was 5V is 0.5 micrometers. It is set to 3.3V in a process generation, and is 0.25 micrometers. It is a well-known

fact that standard actuation supply voltage falls for every generation henceforth [a process generation]. However, as for the peripheral device of a CMOS semiconductor device, 5V system signal from the former and a 3.3V system signal exist. It can consider making the transistor of electrical-potential-difference pressure-proofing which is different in a CMOS semiconductor device for this reason load together. A remarkable part is the gate oxidation thickness and gate length in a MOS transistor in a different part in the configuration of each transistor. On the other hand, the configuration of the bipolar mold transistor in a CMOS semi-conductor process serves as the configuration where the gate of a MOS transistor was deleted. As for actuation of an electrostatic-discharge protection transistor, an MOS mold and a bipolar mold carry out bipolar mold transistor actuation. Here, the gate length who is the parameter defined by the MOS mold is used as the emitter of a bipolar mold transistor, and collector diffusion field spacing. ON state voltage falls, so that in the ON-state-voltage dependency of the transistor to gate length gate length becomes short as is shown by "H.Weston, V.Lee, T.Stanik, 'A Newly Observed High Frequency Effect on the ESD Protection Utilized in a Gigahertz NMOS Technology', in Proc.14 th EOS/ESD Symposium, P.95-98, and 1992." drawing 10 (A) -- 5V a proof-pressure transistor -- gate length LB1 -- 0.6 micrometers drawing 10 (B) -- a 3.3v proof-pressure transistor -- gate length LB2 -- 0.4 micrometers ** -- if it carries out, the potential of an NPN transistor will change from fictitious outlines K1 and K3 to the property of continuous lines K2 and K4 at the business of drawing 10 (C). It is possible to reduce potential about by 1/2 by said data. It becomes possible to reduce the potential difference generated in case a protection component will be energized with constituting the protection component of G25 from a 3.3V proof-pressure transistor, if the supply voltage of VDD1 and VDD3 sets to 3.3V in drawing 1 .

[0061] Thus, two or more circuit fields which have two or more MOS transistor components (drawing 10 (A), (B)) which have two or more electrical-potential-difference pressure-proofing with the gestalt of the 4th operation, and are

operating by different supply voltage network exist, and two or more circuit fields are received. The electrostatic-discharge protection component to at least one supply voltage actuation logical circuit constitutes by the MOS transistor component (drawing 10 (B)) of low-battery pressure-proofing among two or more MOS transistor components (drawing 10 (A), (B)).

[0062] Thereby, when that of the signal level of the semiconductor device circumference does not so much change to the fall of the supply voltage of the semiconductor device by detailed-izing in recent years of operation, it is effectively possible to reduce the potential difference at the time of a protection component energizing using having two electrical-potential-difference pressure-proofing on a semiconductor device having been generalized, and the potential difference rise from the static electricity charge impression terminal to an earth terminal can be lowered.

[0063] In addition, not only a publication but more than it is sufficient as the number of power supply terminals, and also in that case, it can extend the above-mentioned connection relation to the gestalt of each above-mentioned operation, and can be adapted for it. Moreover, a protection component is the diode component or MOS which does not pass the current beyond the leakage current at the time of circuit actuation of a semiconductor device. You may consist of a mold transistor component or a bipolar mold transistor component. Moreover, a protection component may be respectively formed in the bottom of current supply wiring to a supply voltage actuation logical circuit field. Furthermore not only in the MOS transistor component which has two kinds of electrical-potential-difference pressure-proofing but a semiconductor device, the thing using two or more kinds of electrical-potential-difference proof-pressure MOS transistor components is sufficient as a protection component.

[0064]

[Effect of the Invention] According to the semiconductor device according to claim 1, the path which misses impression of the charge by static electricity to an earth terminal is securable by restricting the number of stages of a protection

component, and arranging a protection component, using power-source wiring into an actual circuit effectively.

[0065] According to the semiconductor device according to claim 2, there is the same effectiveness as claim 1.

[0066] According to the semiconductor device according to claim 3, there is the same effectiveness as claim 1.

[0067] According to the semiconductor device according to claim 4, there is the same effectiveness as claim 1.

[0068] When it is the logical circuit configuration which shared one of one electrical power system among many electrical power systems in a semiconductor device according to the semiconductor device according to claim 5, it is possible to reduce a protection element number in addition to the effectiveness of claim 1.

[0069] According to the semiconductor device according to claim 6, there is the same effectiveness as claim 5.

[0070] According to the semiconductor device according to claim 7, there is the same effectiveness as claim 1, claim 2, claim 3, claim 4, claim 5, or claim 6.

[0071] According to the semiconductor device according to claim 8, there is the same effectiveness as claim 1, claim 2, claim 3, claim 4, claim 5, claim 6, or claim 7.

[0072] According to the semiconductor device according to claim 9, it becomes possible to reduce area further by considering the component configuration of a multi-electrical power system protection component as a polygonal mesh configuration.

[0073] According to the semiconductor device according to claim 10, when the signal level of the semiconductor device circumference does not change to the fall of the supply voltage of the semiconductor device by detailed-izing in recent years of operation, it is possible to reduce the potential difference at the time of having two electrical-potential-difference pressure-proofing on a semiconductor device energizing for a protection component, using to have become common

effectively, and the potential difference rise from the static electricity charge impression terminal to an earth terminal can be lowered.

[0074] According to the semiconductor device according to claim 11, there is the same effectiveness as claim 1, claim 2, claim 3, claim 4, claim 5, claim 6, claim 7, claim 8, claim 9, or claim 10.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram showing the gestalt of operation of the 1st of this invention.

[Drawing 2] It is a circuit diagram explaining the deformation gestalt of the gestalt of operation of the 1st of this invention.

[Drawing 3] It is an explanatory view explaining the example which will be the requisite for the gestalt of operation of the 2nd of this invention.

[Drawing 4] It is a circuit diagram explaining the gestalt of operation of the 2nd of this invention.

[Drawing 5] It is an outline sectional view explaining the configuration of a bipolar mold transistor protection component.

[Drawing 6] It is an outline sectional view explaining the configuration of a MOS transistor protection component.

[Drawing 7] It is the Kushigata configuration layout pattern Fig. of a bipolar mold transistor protection component.

[Drawing 8] The layout pattern with which (A) will be the requisite for the gestalt of implementation of the 3rd of the multi-electrical power system Kushigata configuration of a bipolar mold transistor protection component, and (B) are the multi-power-source mesh configuration layout patterns of a bipolar mold transistor protection component, and it is drawing explaining the gestalt of the 3rd operation.

[Drawing 9] It is the enlarged drawing which started a part of layout of drawing 8 (B).

[Drawing 10] The gestalt of the 4th operation is shown, as for (B), (A) shows a transistor with short gate length among MOS transistor protection components by showing a transistor with long inside of a MOS transistor protection component and gate length, (C) is the snapback property of a transistor protection component, and the property difference by the difference in gate length is shown.

[Drawing 11] It is a circuit diagram explaining the conventional example (1).

[Drawing 12] It is a circuit diagram explaining the conventional example (2).

[Description of Notations]

VDD1, VDD2, and ... VDD7, VSS1, VSS2, VSS3, and a VSS4:power system

IN1, IN2, IN3, IN4: Signal input terminal

OUT1, OUT2, OUT3, OUT4: Signal output terminal

IO-P1, IO-P2, and ... IO-P8, IO-N1, IO-N2, and ... the component which constitutes an IO-N8:input signal and an output signal circuit

G1, G2, and ... a G40:electrostatic-discharge protection component

L1, L2, L3, L4: The logical circuit field to which a power source is supplied from each electrical power system

C1: Semiconductor device frame

I1: Internal logical circuit field

n1, n2, and ... an n9:N+ semi-conductor diffusion field

p1, p2, p3 :P + semi-conductor diffusion field

E1: Bipolar mold transistor emitter terminal

C1: Bipolar mold transistor collector terminal

D1: MOS Mold transistor drain terminal

S1: MOS transistor source terminal

Ga1, Ga2 : MOS transistor gate terminal

r1: Substrate resistance

r2: Semiconductor device keepout areas other than a protection component near the protection component

v1, v2: Diffusion field-aluminum wiring contact component

vp1: Gate electrode-aluminum wiring contact component

A, B, C, D, E: A power system / high concentration diffusion field

LB1, LB2: Gate effective length

[Translation done.]

* NOTICES *

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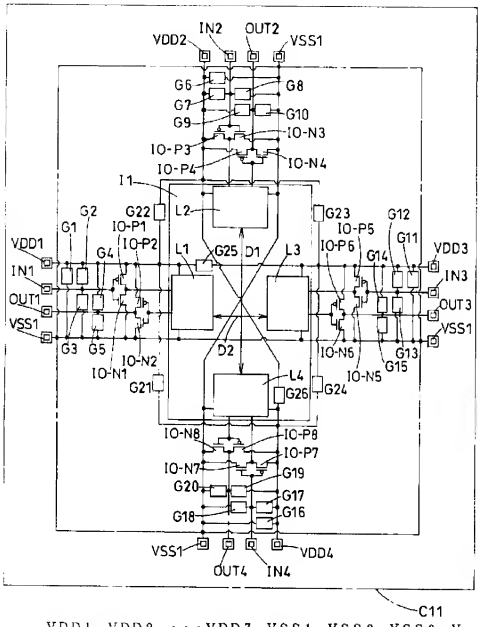
3.In the drawings, any words are not translated.

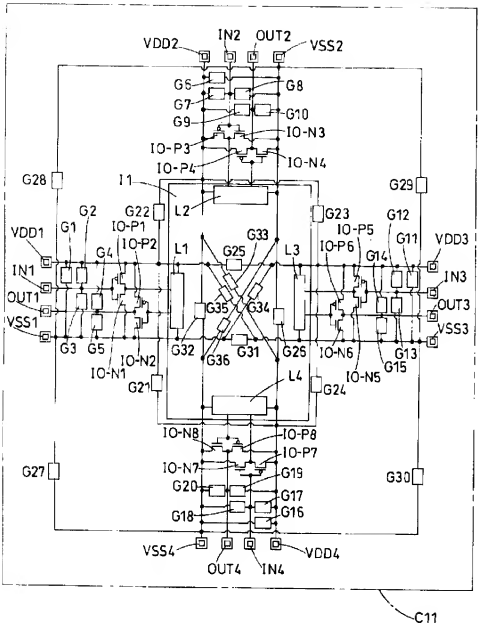
DRAWINGS

[Drawing 1]

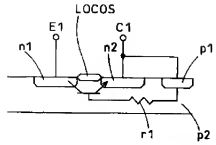


VDD1, VDD2, ・・・VDD7, VSS1, VSS2, VSS3, VSS4…電源系統
IN1, IN2, IN3, IN4…信号入力端子
OUT1, OUT2, OUT3, OUT4…信号出力端子
IO-P1, IO-P2, ・・・IO-P8, IO-N1, IO-N2, ・・・IO-N8…入力信号、出力信号回路を構成する素子
G1, G2, ・・・G38…静電破壊保護素子
L1, L2, L3, L4…各電源系より電源を供給される論理回路領域
C1…半導体装置枠

[Drawing 2]

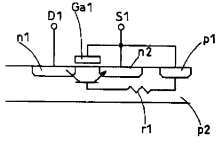

VDD2
IN2
OUT2
VSS2
G6
G8
G7
G10
G9
IO-N3
IO-P3
IO-N4
IO-P4
G28
I1
G29
G2
G22
L2
G23
G12
VDD1
G1
IO-P1
IO-P5
G11
VDD3
IO-P2
G33
IO-P6
G14
IN1
G4
L1
G25
L3
IN3
OUT1
G35
G34
OUT3
VSS1
G3
G5
IO-N2
G32
G31
G25
IO-N6
G13
IO-N1
G36
G15
IO-N5
G21
L4
G24
IO-N8
IO-P8
IO-P7
G27
IO-N7
G19
G30
G20
G17
G18
G16
VSS4
VDD4
OUT4
IN4
C11

[Drawing 5]



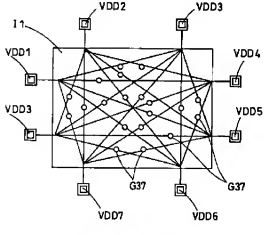
n１，ｎ２，・・・ｎ９…Ｎ－半導体拡散領域
ｐ１，２，ｐ３…Ｐ＋半導体拡散領域
Ｅ１…バイポーラ型トランジスタエミッタ端子
Ｃ１…バイポーラ型トランジスタコレクタ端子

[Drawing 6]



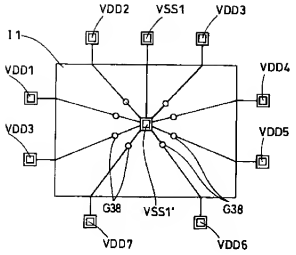
Ｄ１…MOS 型トランジスタドレイン端子
Ｓ１…MOS型トランジスタソース端子

[Drawing 3]

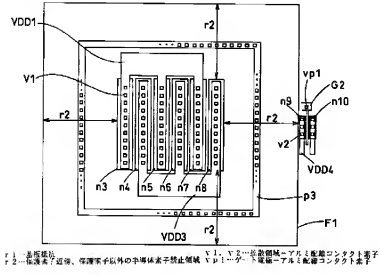


Ｉ１…内部論理回路領域

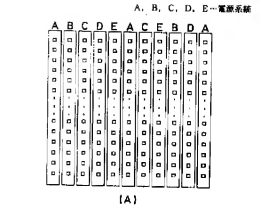
[Drawing 4]

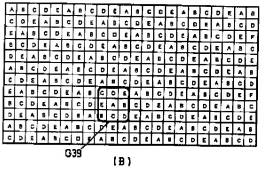


[Drawing 7]

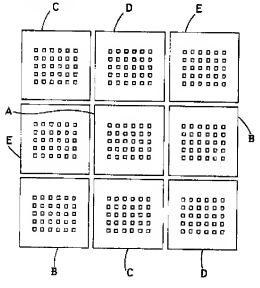


[Drawing 8]

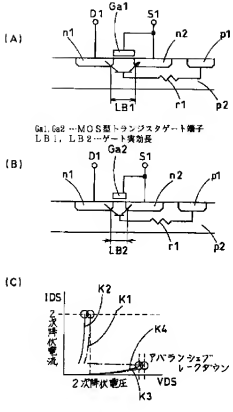




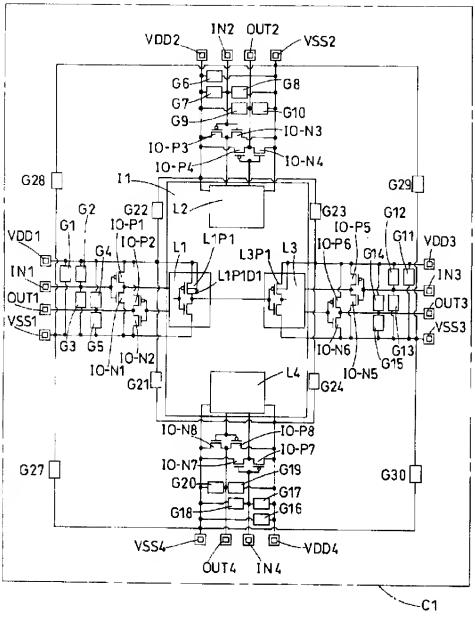
[Drawing 9]



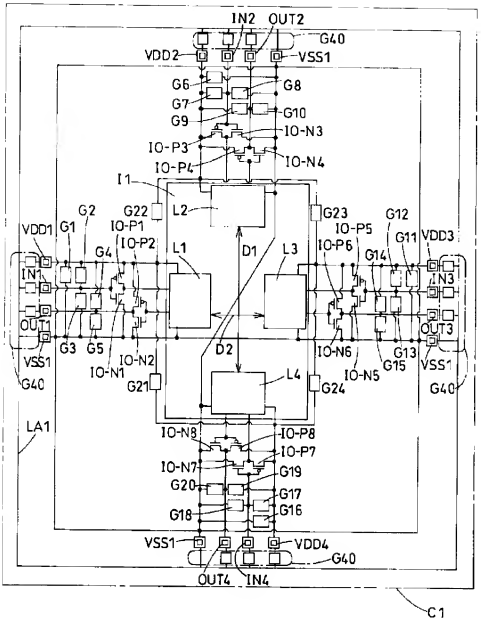
[Drawing 10]


(A)
D1
Ga1
S1
n1
n2
p1
LB1
r1
p2
Ga1, Ga2 …MOS型トランジスタゲート端子
LB1, LB2…ゲート実効長
(B)
D1
Ga2
S1
n1
n2
p1
LB2
r1
p2
(C)
IDS
K2
K1
K4
K3
VDS
2次降伏電流
2次降伏電圧
アバランシェブレークダウン

[Drawing 11]


VDD2
IN2
OUT2
VSS2
G6
G8
G7
G10
G9
IO-N3
IO-P3
IO-N4
IO-P4
G28
I1
G29
G2
G22
L2
G23
G12
G1
IO-P1
IO-P5
VDD1
IO-P2
L1
L1P1
L3P1
L3
IO-P6
G11
VDD3
G4
G14
IN1
L1P1D1
IN3
OUT1
OUT3
VSS1
VSS3
G3
G5
IO-N2
IO-N1
IO-N6
G13
G15
IO-N5
G21
L4
G24
IO-N8
IO-P8
IO-P7
IO-N7
G27
G19
G30
G20
G17
G18
G16
VSS4
VDD4
OUT4
IN4
C1

[Drawing 12]



[Translation done.]